

Parallel Persistent SRAM Memory

(AS3004308, AS3008308, AS3016308, AS3032308)

Features

- Interface
 - Parallel Asynchronous x8
- Technology
 - 40nm pMTJ STT-MRAM
 - Virtually unlimited Endurance and Data Retention (see Endurance and Data Retention on page 20)
- Density
 - 4Mb, 8Mb, 16Mb, 32Mb
- Operating Voltage Range
 - V_{CC} : 2.70V – 3.60V
- Operating Temperature Range
 - Industrial: -40°C to 85°C
 - Industrial Plus: -40°C to 105°C
- RoHS & REACH Compliant
- Packages
 - 44-pin TSOP (10mm x 18mm)
 - 48-ball FBGA (10mm x 10mm)
- Memory Array Organization
 - 4Mbit
 - 524,288 x 8
 - 8Mbit
 - 1,048,576 x 8
 - 16Mbit
 - 2,097,152 x 8
 - 32Mbit
 - 4,194,304 x 8

Performance

| Device Operation | Typical Values | Units |
|------------------|----------------|-------|
| Read Cycle Time | 35.0 (minimum) | ns |
| Write Cycle Time | 35.0 (minimum) | ns |
| Standby Current | 1.7 (typical)* | mA |
| Read Current | 12.0 (typical) | mA |
| Write Current | 20.0 (typical) | mA |

*Number shown is for 16Mb device

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General Description

AS3xxx308 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 4Mbit to 32Mbit. MRAM technology is analogous to Flash technology with SRAM compatible 35ns/35ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution.

Table 1: Technology Comparison

| | SRAM | Flash | EEPROM | MRAM |
|--------------------------|------|-------|--------|------|
| Non-Volatility | – | √ | √ | √ |
| Write Performance | √ | – | – | √ |
| Read Performance | √ | – | – | √ |
| Endurance | √ | – | – | √ |
| Power | – | – | – | √ |

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually unlimited endurance and data retention, high performance and scalable memory technology.

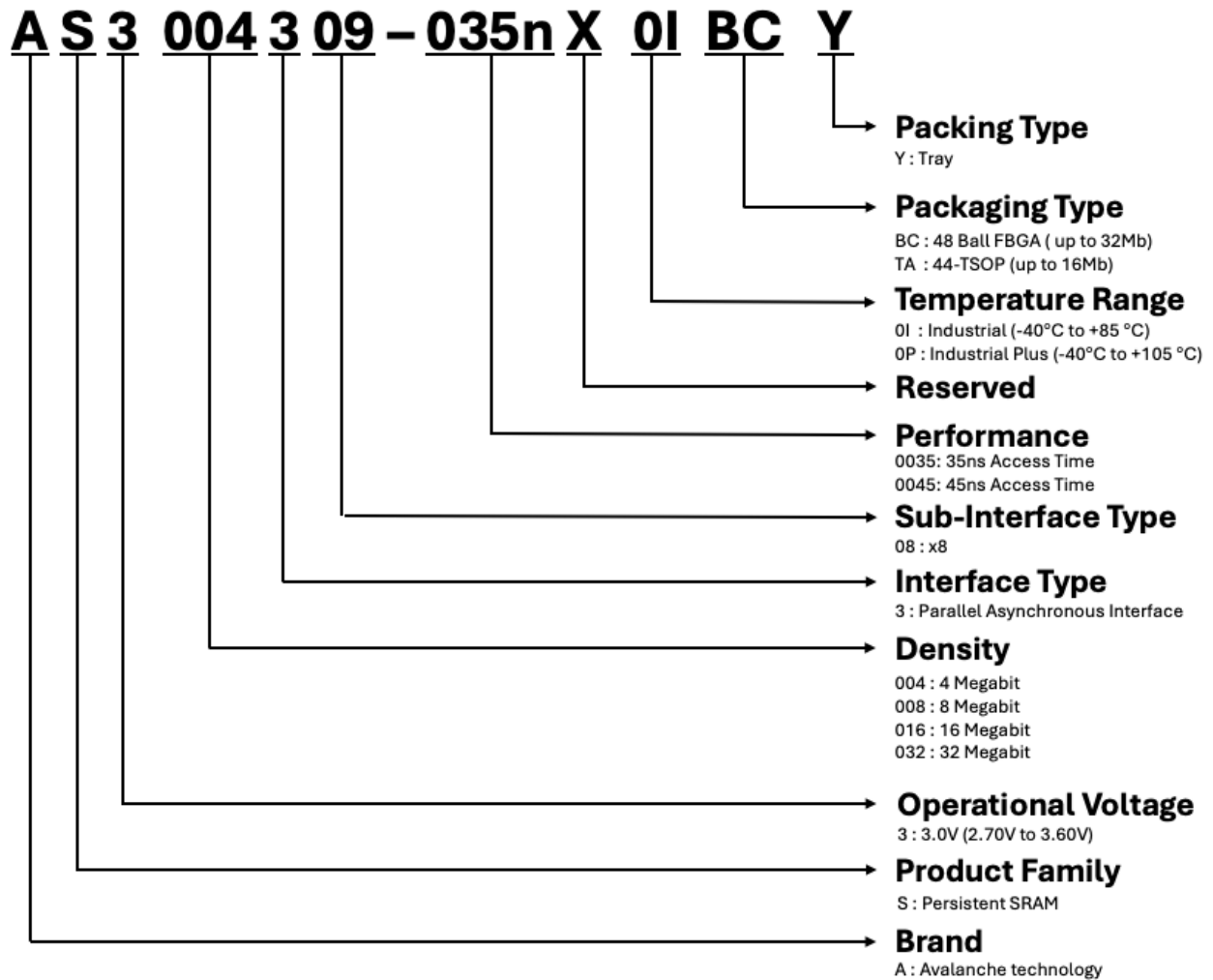
AS3xxx308 is available in small footprint 44-pin TSOP (10mm x 18mm) and 48-ball FBGA (10mm x 10mm) packages. Density of 4Mb is available on the 44-pin TSOP package. Densities ranging from 4Mb to 32Mb are available on the 48-ball FBGA package. These packages are compatible with similar low-power volatile and non-volatile products.

AS3xxx308 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

Figure 1: Part Number Ordering System



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2: Valid Combinations List

| Valid Combinations – 35ns | | | | |
|---------------------------|-------------------|--------------|--------------|----------------------|
| Base Part Number | Temperature Range | Package Type | Packing Type | Part Number |
| AS3004308-035nX | 0I, 0P | BC, TA | Y | AS3004308-035nX0IBCY |
| | | | | AS3004308-035nX0ITAY |
| | | | | AS3004308-035nX0PBCY |
| | | | | AS3004308-035nX0PTAY |
| AS3008308-035nX | 0I, 0P | BC | Y | AS3008308-035nX0IBCY |
| | | | | AS3008308-035nX0PBCY |
| AS3016308-035nX | 0I, 0P | BC | Y | AS3016308-035nX0IBCY |
| | | | | AS3016308-035nX0PBCY |
| AS3032308-035nX | 0I, 0P | BC | Y | AS3032308-035nX0IBCY |
| | | | | AS3032308-035nX0PBCY |

| Valid Combinations – 45ns | | | | |
|---------------------------|-------------------|--------------|--------------|----------------------|
| Base Part Number | Temperature Range | Package Type | Packing Type | Part Number |
| AS3004308-045nX | 0I, 0P | BC, TA | Y | AS3004308-045nX0IBCY |
| | | | | AS3004308-045nX0ITAY |
| | | | | AS3004308-045nX0PBCY |
| | | | | AS3004308-045nX0PTAY |
| AS3008308-045nX | 0I, 0P | BC | Y | AS3008308-045nX0IBCY |
| | | | | AS3008308-045nX0PBCR |
| AS3016308-045nX | 0I, 0P | BC | Y | AS3016308-045nX0IBCY |
| | | | | AS3016308-045nX0PBCY |
| AS3032308-045nX | 0I, 0P | BC | Y | AS3032308-045nX0IBCY |
| | | | | AS3032308-045nX0PBCY |

Signal Description and Assignment

Figure 2: Device Pinout

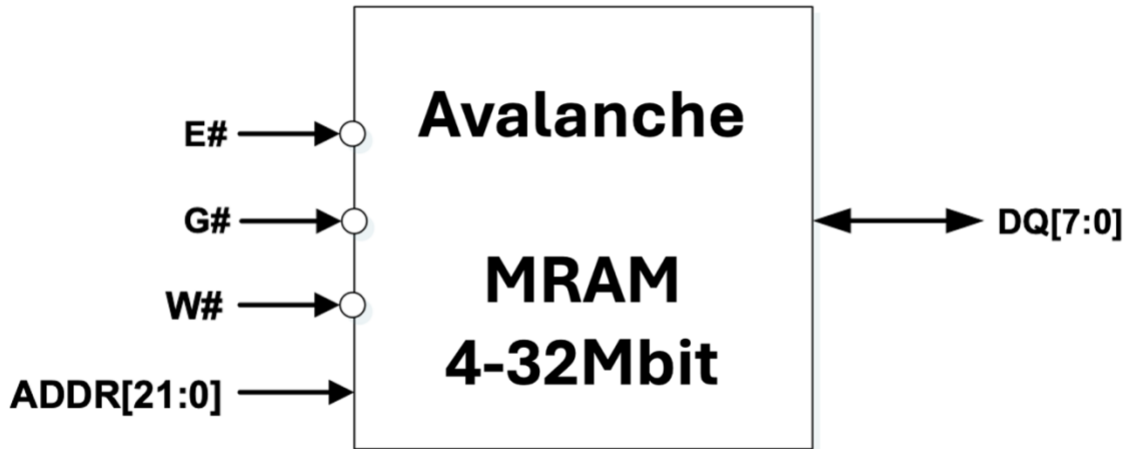
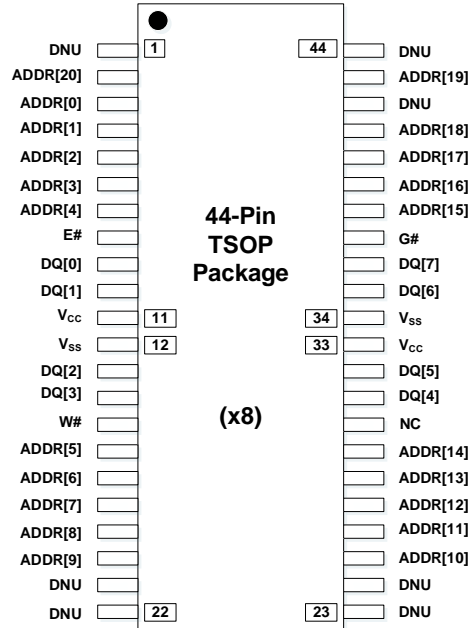


Table 3: Signal Description

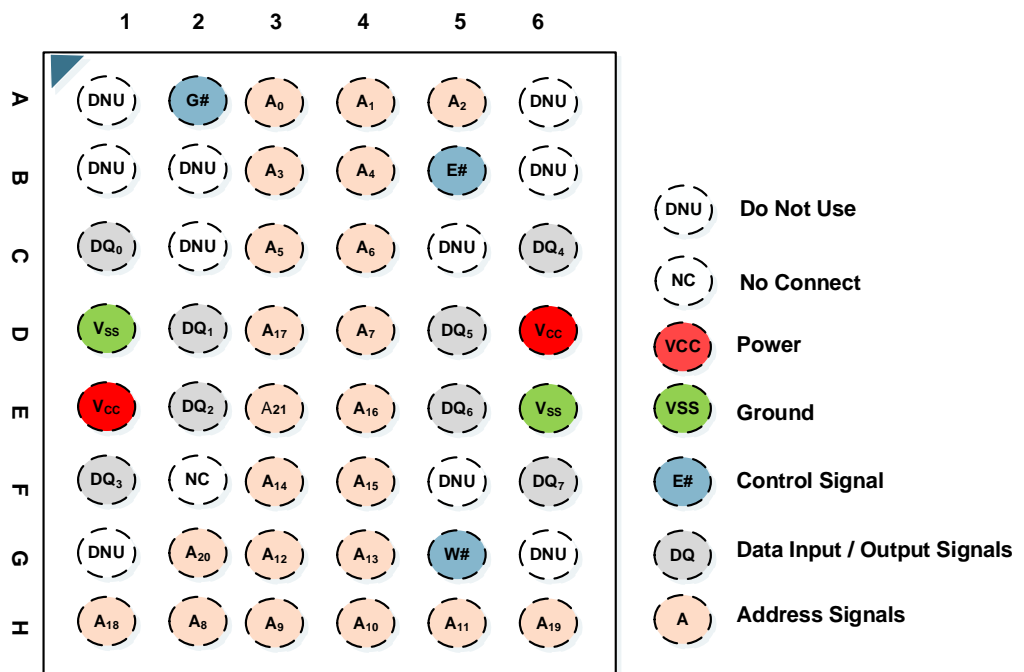
| Signal | Type | Description |
|-----------------|----------------|---|
| E# | Input | Chip enable: Enables or disables the MRAM. |
| G# | Input | Output enable: Enables the output drivers in bidirectional data transfer I/Os. |
| W# | Input | Write enable: Transfers data from the host system to the MRAM when Low (Logic '0'). Transfers data from the MRAM to the host system when High (Logic '1'). |
| ADDR[21:0] | Input | Address: I/Os for address transfer. 04M: ADDR[18:0] – 19 Address pins for 04M devices. 08M: ADDR[19:0] – 20 Address pins for 08M devices. 16M: ADDR[20:0] – 21 Address pins for 16M devices. 32M: ADDR[21:0] – 22 Address pins for 32M devices (48-ball FBGA only) |
| DQ[7:0] | Input / Output | Data inputs/outputs: The bidirectional I/Os transfer data. |
| V _{cc} | Supply | V_{cc}: Core and I/O power supply. |
| V _{ss} | Supply | V_{ss}: Core and I/O ground supply. |
| NC | | No connect: NCs are not internally connected. They can be driven or left unconnected. |
| DNU | | Do not use: DNUs must be left unconnected. |

Package Options

44-Pin TSOP (4-16Mb) (Top View)

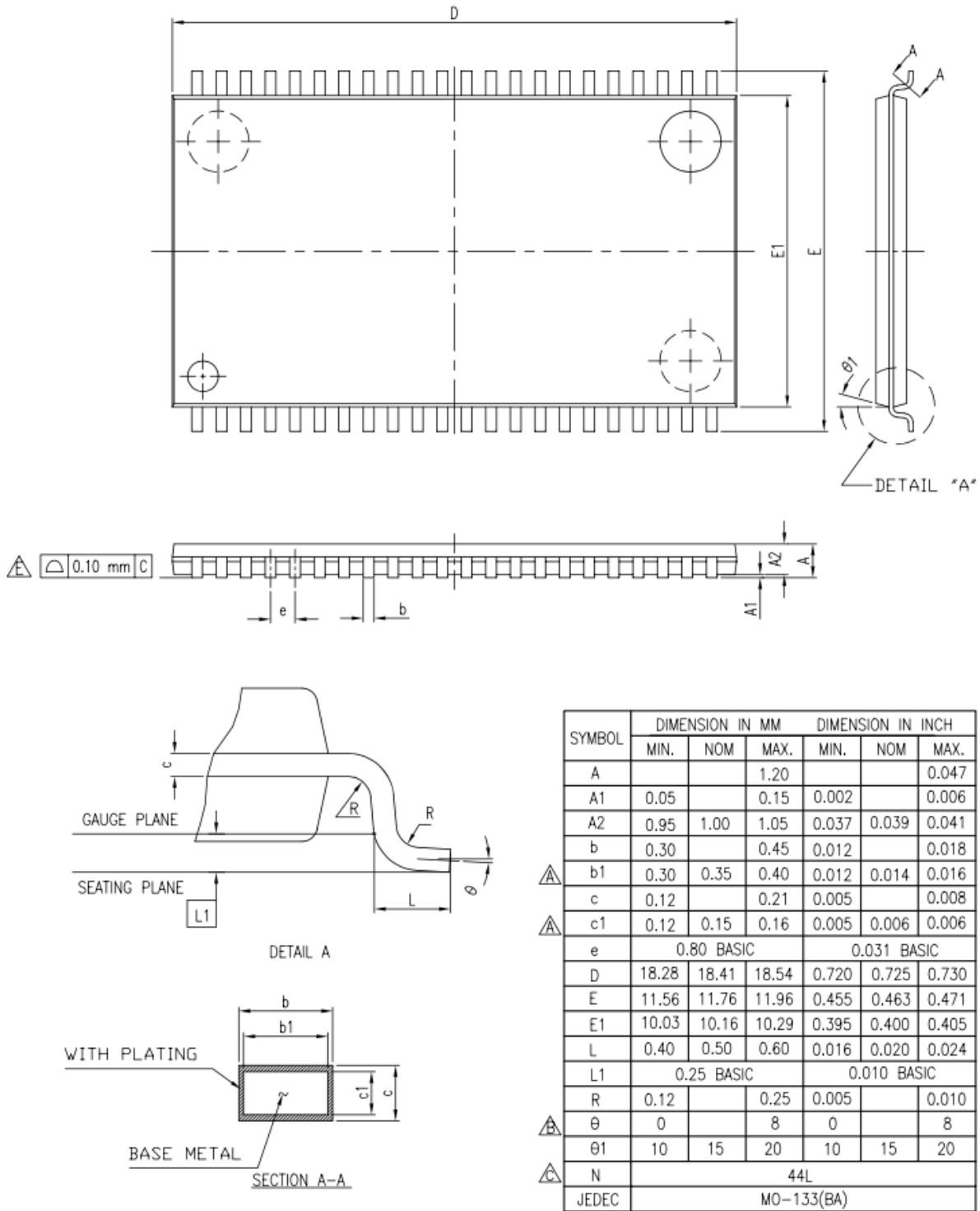


48-Ball FBGA (4-32Mb) (Balls Down, Top View)



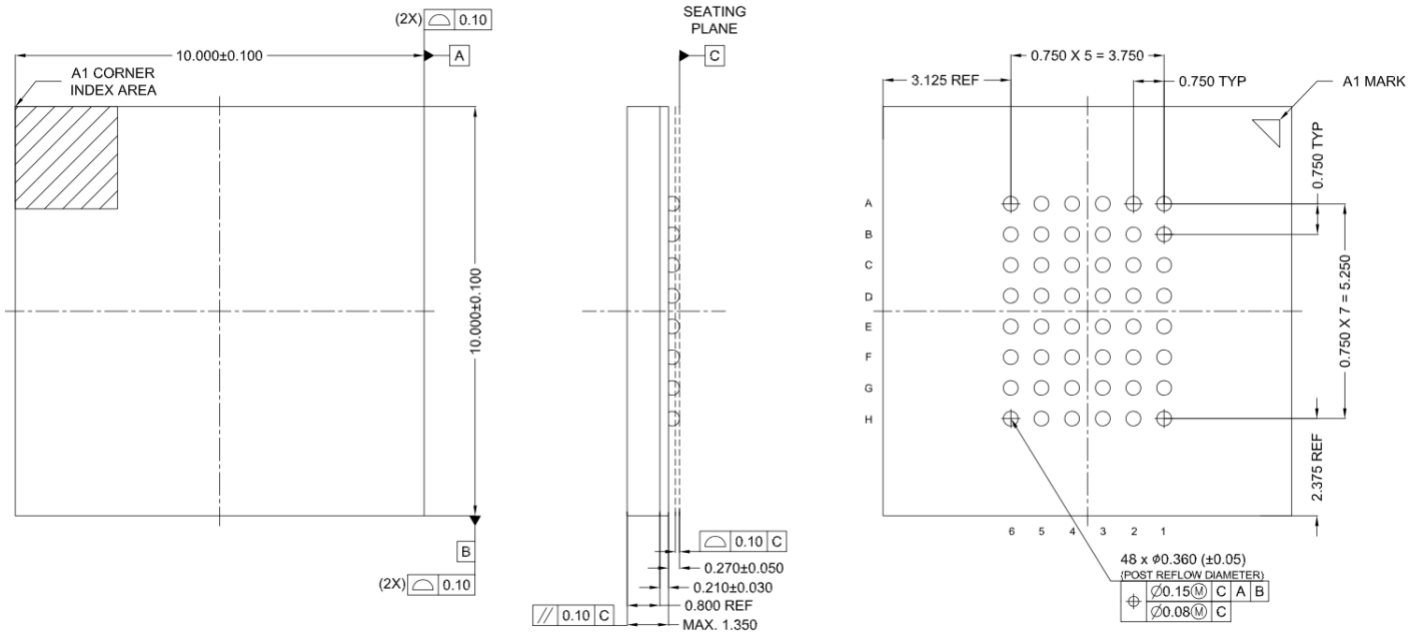
Package Drawings

44-Pin TSOP



NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.
 D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

48-Ball FBGA



Architecture

AS3xxx308 is a high performance MRAM device. Writing to and reading from the device are performed as follows:

To write to the device, bring Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[7]) to be written into the memory location specified by the address pins (ADDR[0] through ADDR[20] on the 44-pin TSOP and through ADDR[21] on the 48-ball FBGA).

To read from the device, bring Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins (ADDR[0] through ADDR[20] on the 44-pin TSOP and ADDR[21] on the 48-ball FBGA) to appear on I/O pins (DQ[0] to DQ[7]).

Figure 3: Functional Block Diagram

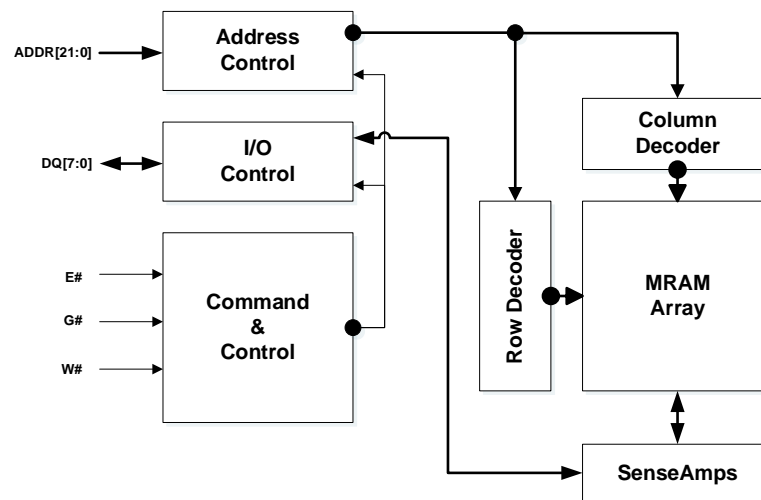


Table 4: Modes of Operation

| Mode | E# | G# | W# | Current | DQ[7:0] |
|-----------------|----|----|----|--------------------|---------|
| Not Selected | H | X | X | I _{SB} | Hi-Z |
| Output Disabled | L | H | H | I _{READ} | Hi-Z |
| Read | L | L | H | I _{READ} | Dataout |
| Write | L | X | L | I _{WRITE} | Datain |

Notes:

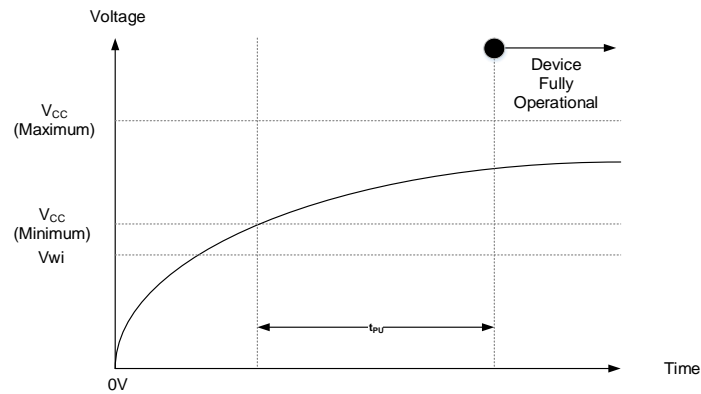
H: High (Logic '1')
 L: Low (Logic '0')
 X: Don't Care
 Hi-Z: High Impedance

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- E#, W#, G# must follow V_{CC} during power-up

Figure 4: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G# must follow V_{CC} during power-down
- During power loss or brownout, where V_{CC} goes below V_{wi} , read/write operations are prohibited. The power-up timing needs to be observed after V_{CC} goes above V_{CC} (minimum)

Figure 5: Power-Down Behavior

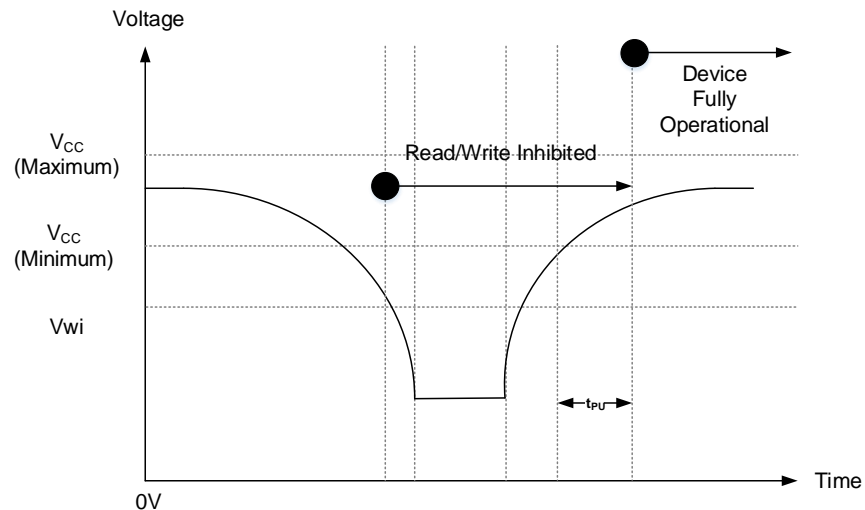


Table 6: Device Initialization Timing – 3.0V

| Parameter | Symbol | Test Conditions | 3.0V | | | Units |
|---|-----------------|---|---------|---------|---------|-------|
| | | | Minimum | Typical | Maximum | |
| V_{CC} Range | | All operating voltages and temperatures | 2.7 | - | 3.6 | V |
| V_{CC} Power Up to First Instruction | t _{PU} | All operating voltages and temperatures | 1 | - | - | ms |

Electrical Specifications

Table 7: Recommended Operating Conditions

| Parameter / Condition | Minimum | Typical | Maximum | Units | |
|---------------------------------------|-----------------|---------|---------|-------|----|
| | Industrial | -40.0 | - | 85.0 | °C |
| | Industrial Plus | -40.0 | - | 105.0 | °C |
| V _{CC} Supply Voltage | 3.0V | 2.7 | 3.0 | 3.6 | V |
| V _{SS} Supply Voltage | | 0.0 | 0.0 | 0.0 | V |
| V _{wi} Write Inhibit Voltage | | 2.1 | 2.3 | 2.5 | V |

Table 8: Pin Capacitance

| Parameter | Symbol | Test Conditions | Density | Maximum | Units |
|--------------------------------|--------------------|---|---------|---------|-------|
| Input Pin Capacitance | C _{IN} | TEMP = 25°C; f = 1 MHz; V _{IN} = 0V | 4-16Mb | 10.0 | pF |
| | | | 32b | 20.0 | |
| Input / Output Pin Capacitance | C _{INOUT} | TEMP = 25°C; f = 1 MHz; V _{IN} = 0V | 4-16Mb | 10.0 | pF |
| | | | 32Mb | 20.0 | |

Table 9: DC Characteristics

| Parameter | Symbol | Test Conditions | 3.0V Device (2.7V-3.6V) | | | Units | |
|--|--------------------|---|-------------------------|----------------------|---------|----------------------|----|
| | | | Minimum | Typical | Maximum | | |
| Read Current | I _{READ} | V _{CC} (max), I _{OUT} =0mA | 4 – 32Mb | - | 12.0 | 30.0 | mA |
| Write Current | I _{WRITE} | V _{CC} (max) | 4 – 32Mb | - | 20.0 | 30.0 | mA |
| Standby Current Industrial (-40°C to 85°C) | I _{SB} | E#=V _{IH} , V _{CC} (max) | 4-16Mb | - | 1.5 | 2.5 | mA |
| | | | 32Mb | | 3.0 | 5.0 | |
| Standby Current Industrial Extended (-40°C to 105°C) | I _{SB} | E#=V _{IH} , V _{CC} (max) | 4 -16Mb | - | 1.7 | 3.5 | mA |
| | | | 32Mb | | 3.4 | 7.0 | |
| Input Leakage Current | I _{LI} | V _{IN} =0 to V _{CC} (max) | | - | - | ±1.0 | µA |
| Output Leakage Current | I _{LO} | V _{OUT} =0 to V _{CC} (max) | | - | - | ±1.0 | µA |
| Input High Voltage | V _{IH} | | | 0.8xV _{CC} | - | V _{CC} +0.3 | V |
| Input Low Voltage | V _{IL} | | | -0.5 | - | 0.2xV _{CC} | V |
| Output High Voltage Level | V _{OH} | I _{OH} = -1.6mA | | V _{CC} -0.5 | - | - | V |
| Output Low Voltage Level | V _{OL} | I _{OL} = 1.6mA | | - | - | 0.4 | V |

Table 10: Magnetic Immunity Characteristics

| Parameter | Symbol | Maximum | Units |
|-----------------------------|-------------------|---------|-------|
| Magnetic Field During Write | H_{\max_write} | 24000 | A/m |
| Magnetic Field During Read | H_{\max_read} | 24000 | A/m |

Table 11: AC Test Conditions

| Parameter | Value |
|--|------------------|
| Input pulse levels | 0.0V to V_{CC} |
| Input rise and fall times | 5ns |
| Input and output measurement timing levels | $V_{CC}/2$ |
| Output Load | CL = 30pF |

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

Table12: Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Units |
|---|------------|-----------|-------|
| Magnetic Field During Write | --- | 24000 | A/m |
| Magnetic Field During Read | --- | 24000 | A/m |
| Junction Temperature | --- | 125 | °C |
| Storage Temperature | -55 to 150 | | °C |
| Supply Voltage Vcc relative to Vss | -0.5 | 4.0 | V |
| Voltage on any pin | -0.5 | Vcc + 0.4 | V |
| DC output current Iout | ± 20 | | mA |
| ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017 | ≥ 2000 V | | V |
| ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018 | ≥ 500 V | | V |
| Latch-Up (I-test) JESD78 | ≥ 100 mA | | mA |
| Latch-Up (Vsupply over-voltage test) JESD78 | Passed | | --- |

Write Operation

Figure 7: Write Operation (W# Controlled)

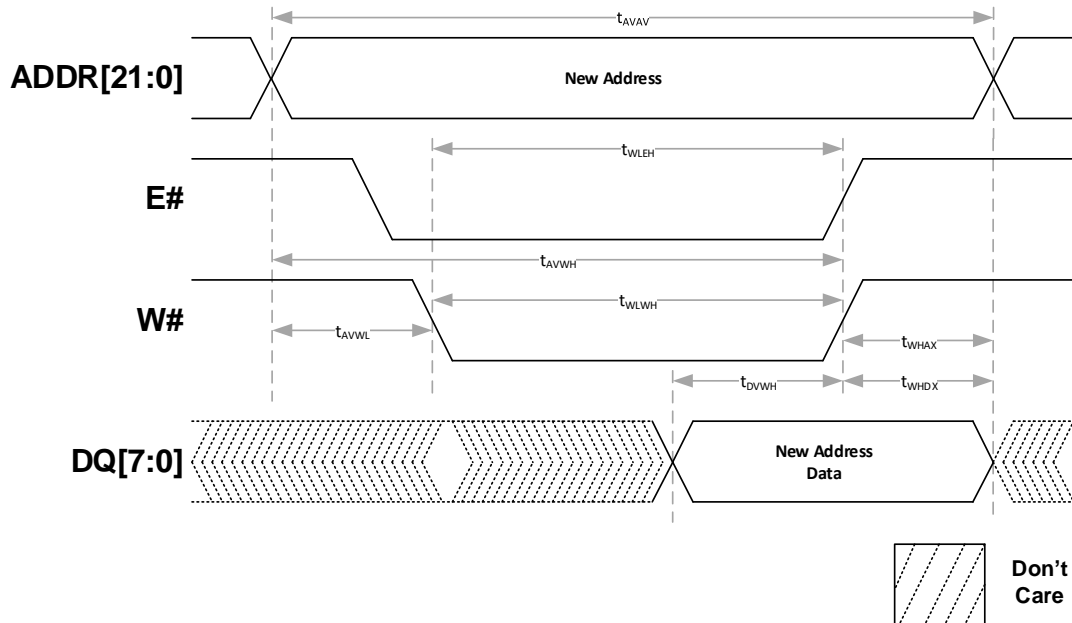


Table 13: Write Operation (W# Controlled)

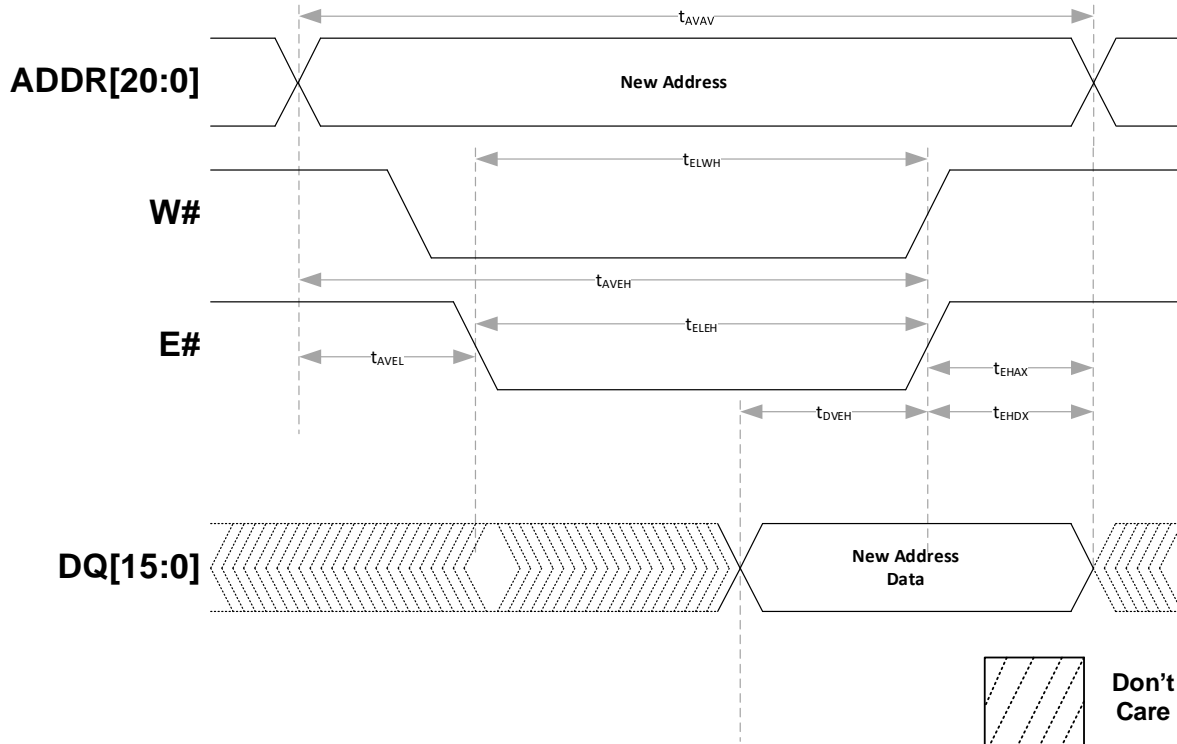
| Parameter | Symbol | Minimum | | Maximum | Units |
|---|----------------------|---------|------|---------|-------|
| | | 35ns | 45ns | | |
| Write Cycle Time | t_{AVAV} | 35 | 45 | - | ns |
| Address Set-Up Time | t_{AVWL} | 0 | | - | ns |
| Address Valid to end of Write (G# High) | t_{AVWH} | 18 | 28 | - | ns |
| Address Valid to end of Write (G# Low) | t_{AVWH} | 20 | 30 | - | ns |
| Write Pulse Width (G# High) | t_{WLWH}, t_{WLEH} | 15 | 25 | - | ns |
| Write Pulse Width (G# Low) | t_{WLWH}, t_{WLEH} | 15 | 25 | - | ns |
| Data Valid to end of Write | t_{DVWH} | 10 | 15 | - | ns |
| Data Hold Time | t_{WHDX} | 0 | | - | ns |
| Write recovery Time | t_{WHAX} | 12 | | - | ns |

Notes:

G# is High (Logic '1') for Write operation

Power supplies must be stable

Addresses valid either before or at the same time as $E\#$ goes low

Figure 8: Write Operation (E# Controlled)

Table 14: Write Operation (E# Controlled)

| Parameter | Symbol | Minimum | | Maximum | Units |
|---|----------------------|---------|------|---------|-------|
| | | 35ns | 45ns | | |
| Write Cycle Time | t_{AVAV} | 35 | 45 | - | ns |
| Address Set-Up Time | t_{AVEL} | 0 | | - | ns |
| Address Valid to end of Write (G# High) | t_{AVEH} | 18 | 28 | - | ns |
| Address Valid to end of Write (G# Low) | t_{AVEH} | 20 | 30 | - | ns |
| Write Pulse Width (G# High) | t_{ELWH}, t_{ELEH} | 15 | 25 | - | ns |
| Write Pulse Width (G# Low) | t_{ELWH}, t_{ELEH} | 15 | 25 | - | ns |
| Data Valid to end of Write | t_{DVEH} | 10 | 15 | - | ns |
| Data Hold Time | t_{EHDX} | 0 | | - | ns |
| Write recovery Time | t_{EHAX} | 12 | | - | ns |

Notes:

G# is High (Logic '1') for Write operation

Power supplies must be stable

Addresses valid either before or at the same time as W# goes low

Bus Turnaround Operation – Read to Write

Figure 9: Bus Turnaround Operation

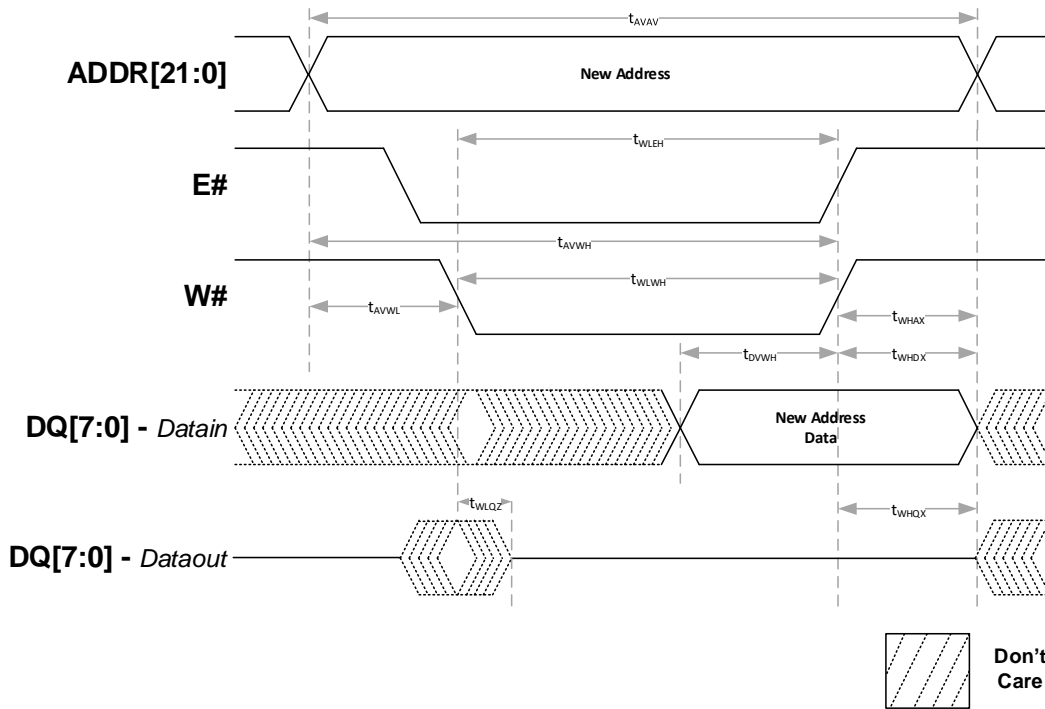


Table 15: Bus Turnaround

| Parameter | Symbol | Minimum | Maximum | | Units |
|--------------------------|------------|---------|---------|------|-------|
| | | | 35ns | 45ns | |
| W# Low to Data Hi-Z | t_{WLQZ} | 0 | 12 | 15 | ns |
| W# High to Output Active | t_{WHQX} | 3 | - | - | ns |

Notes:

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

Read Operation

Figure 10: Read Operation

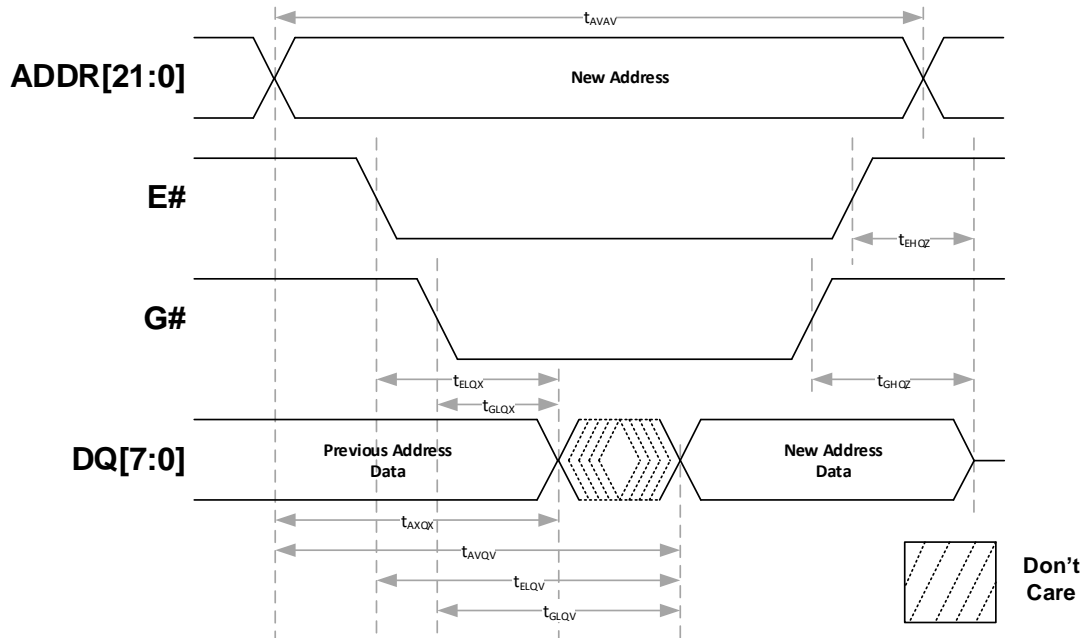


Table 16: Read Operation

| Parameter | Symbol | Minimum | | Maximum | | Units |
|------------------------------------|------------|---------|------|---------|------|-------|
| | | 35ns | 45ns | 35ns | 45ns | |
| Read Cycle Time | t_{AVAV} | 35 | 45 | - | - | ns |
| Address Cycle Time | t_{AVQV} | - | - | 35 | 45 | ns |
| Chip Enable Access Time | t_{ELQV} | - | - | 35 | 45 | ns |
| Output Enable Access Time | t_{GLQV} | - | - | 15 | 25 | ns |
| Byte Enable Access Time | t_{BLQV} | - | - | 15 | 25 | ns |
| Output Hold From Address Change | t_{AXQX} | 3 | - | - | - | ns |
| Chip Enable Low to Output Active | t_{ELQX} | 3 | - | - | - | ns |
| Output Enable Low to Output Active | t_{GLQX} | 0 | - | - | - | ns |
| Byte Enable Low to Output Active | t_{BLQX} | 0 | - | - | - | ns |
| Chip Enable High to Output Hi-Z | t_{EHQZ} | 0 | - | 15 | - | ns |
| Output Enable High to Output Hi-Z | t_{GHQZ} | 0 | - | 10 | 15 | ns |
| Byte Enable High to Output Hi-Z | t_{BHQZ} | 0 | - | 10 | - | ns |

Notes:

W# is High (Logic '1') for Read operation

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

Endurance and Data Retention

Table 17: Endurance & Data Retention

| Parameter | Symbol | Test Conditions | Minimum | Units |
|------------------------|--------|-----------------|------------------|--------|
| Write Endurance | END | - | 10 ¹⁴ | cycles |
| Data Retention | RET | 105°C | 10 | years |
| | | 85°C | 1,000 | |
| | | 75°C | 10,000 | |
| | | 65°C | 1,000,000 | |

Thermal Resistance

Table 18: Thermal Resistance

| Parameter | Description | Test Conditions | 44-pin TSOP (4Mb) | 48 Ball FBGA (4-16Mb) | 48 Ball FBGA (32Mb) | Unit |
|---------------|--|---|-------------------|-----------------------|---------------------|------|
| θ_{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 40.05 | 42.67 | 43.98 | °C/W |
| θ_{JC} | Thermal resistance (junction to case) | | 7.02 | 11.09 | 11.82 | |

Notes:

1: These parameters are guaranteed by characterization; not tested in production.

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Revision History

| Revision | Date | Change Summary |
|--------------|--|--|
| REV Q | 12/01/2020 | Updated Package Drawings – 44-Pin TSOP and 48-Ball FBGA Removed “Preliminary” from the footer. |
| REV R | 07/16/2021 | Removed Sleep mode SE# functionality. This function has been removed to be 100% functionally compatible with legacy devices. The previously assigned Pin or Ball is now designated as “NC”. Removed UB# and LB# from Timing diagram as it does not apply to 8 bit devices. Added pin capacitance for 32Mb Updated DC Characteristics Updated Product Use Limitations |
| REV T | 04/18/2022 05/09/2022 05/18/2022 | Skipped REV S. Added Absolute Maximum Ratings Table Corrected Table 6 : V _{CC} Power Up to First Instruction = 1ms Fixed Spelling Mistake |
| REV U | 07/30/2024 07/31/2024 | Removed 1Mb density option. Removed Tape and Reel Packing type option. TSOP density limited to 4Mb option. |