

# Parallel Persistent SRAM Memory

(AS3004316, AS3008316, AS3016316, AS3032316)

## Features

- Interface
  - Parallel Asynchronous x16
- Technology
  - 40nm pMTJ STT-MRAM
  - Virtually unlimited Endurance and Data Retention (see Endurance and Data Retention on page 22)
- Density
  - 4Mb, 8Mb, 16Mb, 32Mb
- Operating Voltage Range
  - $V_{CC}$ : 2.70V – 3.60V
- Operating Temperature Range
  - Industrial: -40°C to 85°C
  - Industrial Plus: -40°C to 105°C
- RoHS & REACH Compliant
- Packages
  - 44-pin TSOP (10mm x 18mm)
  - 48-ball FBGA (10mm x 10mm)
- Memory Array Organization
  - 4Mbit
    - 262,144 x 16
  - 8Mbit
    - 524,288 x 16
  - 16Mbit
    - 1,048,576 x 16
  - 32Mbit
    - 2,097,152 x 16

## Performance

Device Operation	Typical Values	Units
Read Cycle Time	35.0 (minimum)	ns
Write Cycle Time	35.0 (minimum)	ns
Standby Current	1.7 (typical)*	mA
Read Current	12.0 (typical)	mA
Write Current	20.0 (typical)	mA

\*Number shown is for 16Mb device

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## General Description

AS3xxx316 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 4Mbit to 32Mbit. MRAM technology is analogous to Flash technology with SRAM compatible 35ns/35ns and 45ns/45ns read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile. This makes MRAM a very reliable and fast non-volatile memory solution.

**Table 1: Technology Comparison**

	SRAM	Flash	EEPROM	MRAM
<b>Non-Volatility</b>	–	√	√	√
<b>Write Performance</b>	√	–	–	√
<b>Read Performance</b>	√	–	–	√
<b>Endurance</b>	√	–	–	√
<b>Power</b>	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, virtually unlimited endurance and data retention, high performance and scalable memory technology.

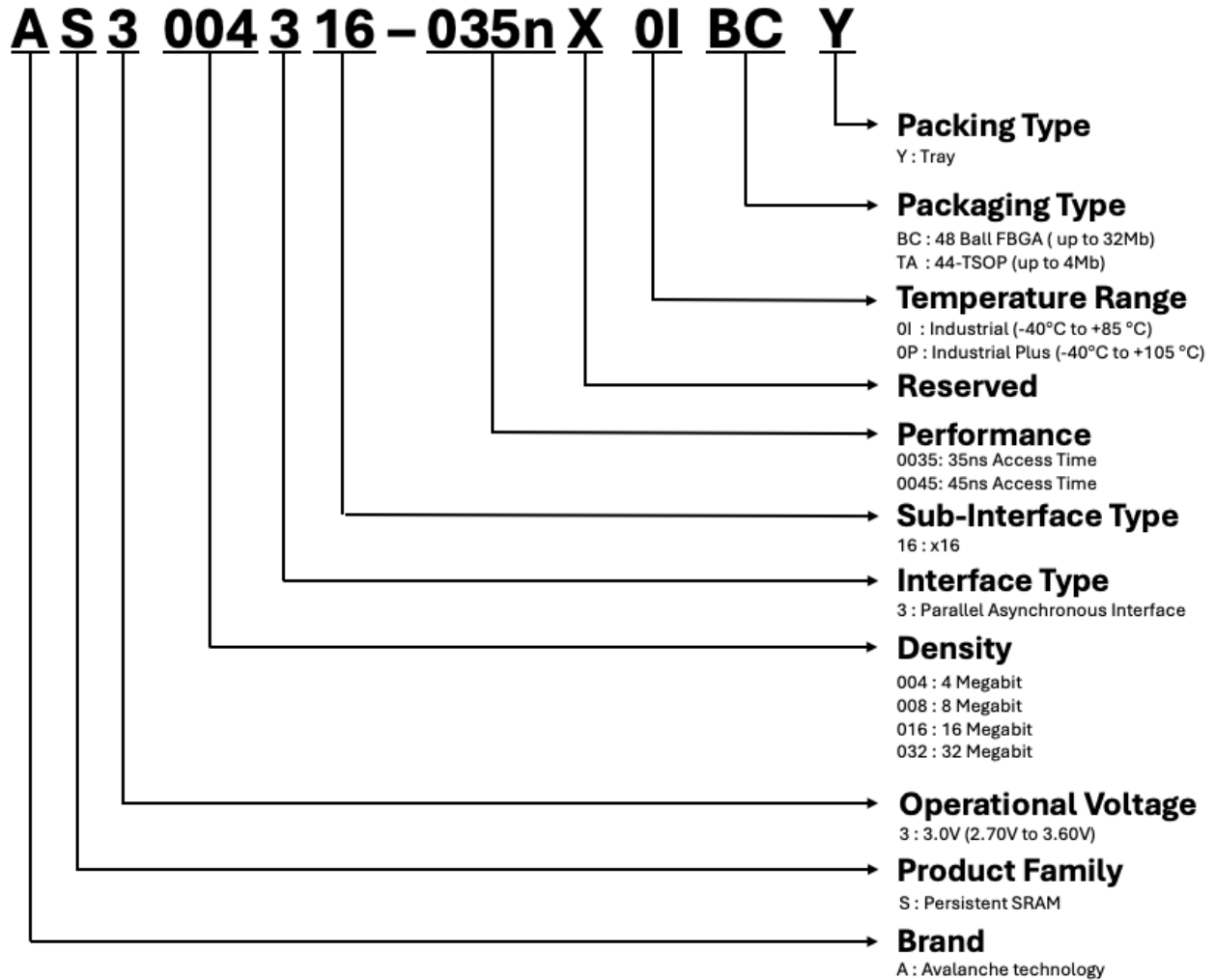
AS3xxx316 is available in small footprint 48-Ball FBGA (10mm x 10mm) packages supporting densities ranging from 4Mb to 32Mb. Density of 4Mb is also available in a small footprint 44-pin TSOP (10mm x 18mm). These packages are compatible with similar low-power volatile and non-volatile products.

AS3xxx316 is offered with industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

## Ordering Options

The ordering part numbers are formed by a valid combination of the following options:

*Figure 1: Part Number Ordering System*



## Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

**Table 2: Valid Combinations List**

Valid Combinations – 35ns				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
AS3004316-035nX	0I, 0P	BC, TA	Y	AS3004316-035nX0IBCY
				AS3004316-035nX0ITAY
				AS3004316-035nX0PBCY
				AS3004316-035nX0PTAY
AS3008316-035nX	0I, 0P	BC	Y	AS3008316-035nX0IBCY
				AS3008316-035nX0PBCY
AS3016316-035nX	0I, 0P	BC	Y	AS3016316-035nX0IBCY
				AS3016316-035nX0PBCY
AS3032316-035nX	0I, 0P	BC	Y	AS3032316-035nX0IBCY
				AS3032316-035nX0PBCY

Valid Combinations – 45ns				
Base Part Number	Temperature Range	Package Type	Packing Type	Part Number
AS3004316-045nX	0I, 0P	BC, TA	Y	AS3004316-045nX0IBCY
				AS3004316-045nX0ITAY
				AS3004316-045nX0PBCY
				AS3004316-045nX0PTAY
AS3008316-045nX	0I, 0P	BC	Y	AS3008316-045nX0IBCY
				AS3008316-045nX0PBCY
AS3016316-045nX	0I, 0P	BC	Y	AS3016316-045nX0IBCY
				AS3016316-045nX0PBCY
AS3032316-045nX	0I, 0P	BC	Y	AS3032316-045nX0IBCY
				AS3032316-045nX0PBCY

## Signal Description and Assignment

Figure 2: Device Pinout

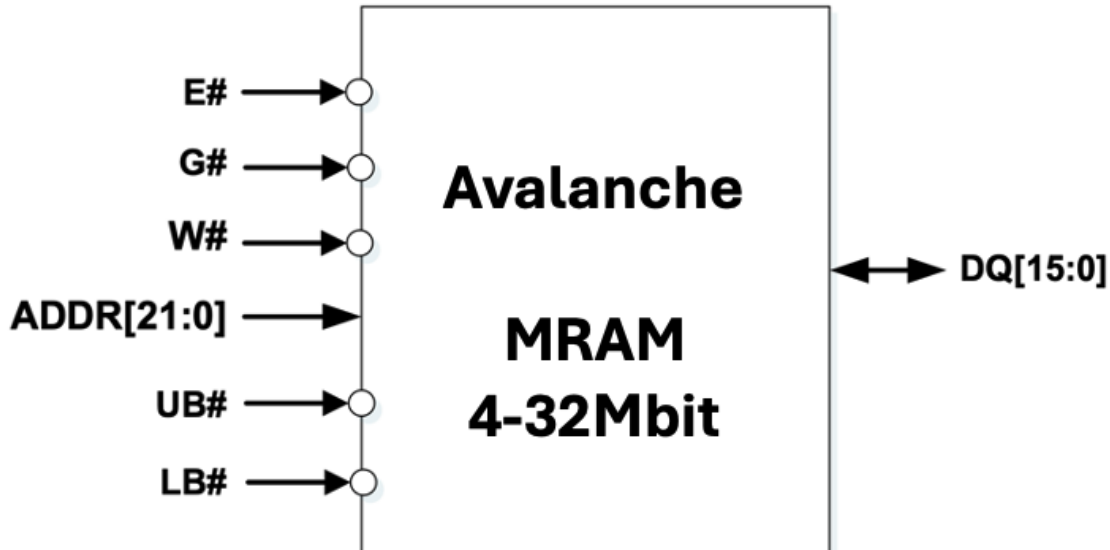


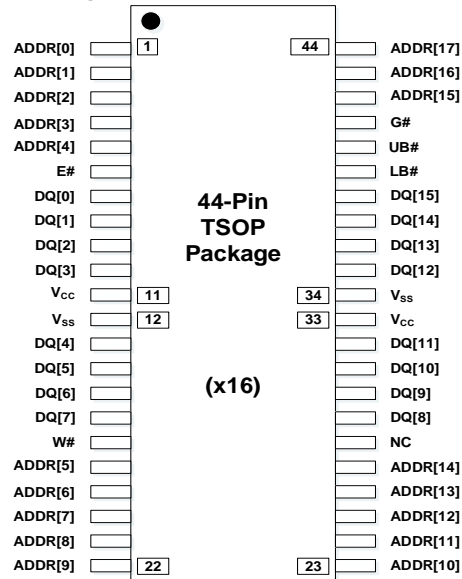
Table 3: Signal Description

Signal	Type	Description
<b>E#</b>	Input	<b>Chip enable:</b> Enables or disables the MRAM.
<b>G#</b>	Input	<b>Output enable:</b> Enables the output drivers in bidirectional data transfer I/Os.
<b>W#</b>	Input	<b>Write enable:</b> Transfers serial data from the host system to the MRAM when Low (Logic '0'). Transfers serial data from the MRAM to the host system when High (Logic '1').
<b>UB#</b>	Input	<b>Upper Byte Enable:</b> Enables or disables DQ[15:8].
<b>LB#</b>	Input	<b>Lower Byte Enable:</b> Enables or disables DQ[7:0].
<b>ADDR[20:0]</b>	Input	<b>Address:</b> I/Os for address transfer. 01M: ADDR[15:0] – 16 Address pins for 01M devices. 04M: ADDR[17:0] – 18 Address pins for 04M devices. 08M: ADDR[18:0] – 19 Address pins for 08M devices. 16M: ADDR[19:0] – 20 Address pins for 16M devices. 32M: ADDR[20:0] – 21 Address pins for 32M devices.
<b>DQ[15:0]</b>	Input / Output	<b>Data inputs/outputs:</b> The bidirectional I/Os transfer data.
<b>V<sub>cc</sub></b>	Supply	<b>V<sub>cc</sub>:</b> Core and I/O power supply.
<b>V<sub>ss</sub></b>	Supply	<b>V<sub>ss</sub>:</b> Core and I/O ground supply.

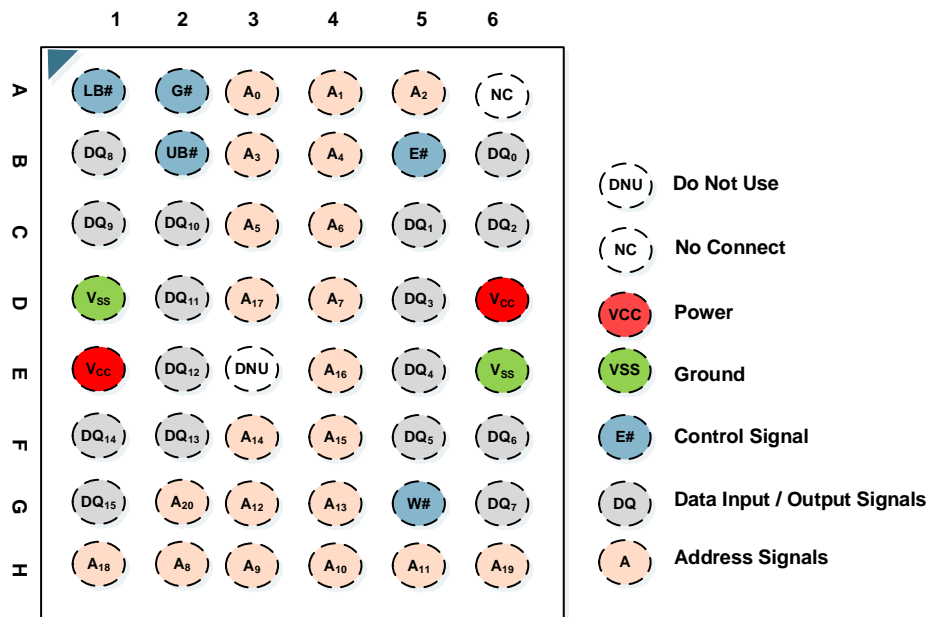
<b>NC</b>		<b>No connect:</b> NCs are not internally connected. They can be driven or left unconnected.
<b>DNU</b>		<b>Do not use:</b> DNUs must be left unconnected.

## Package Options

### 44-Pin TSOP (4Mb) (Top View)



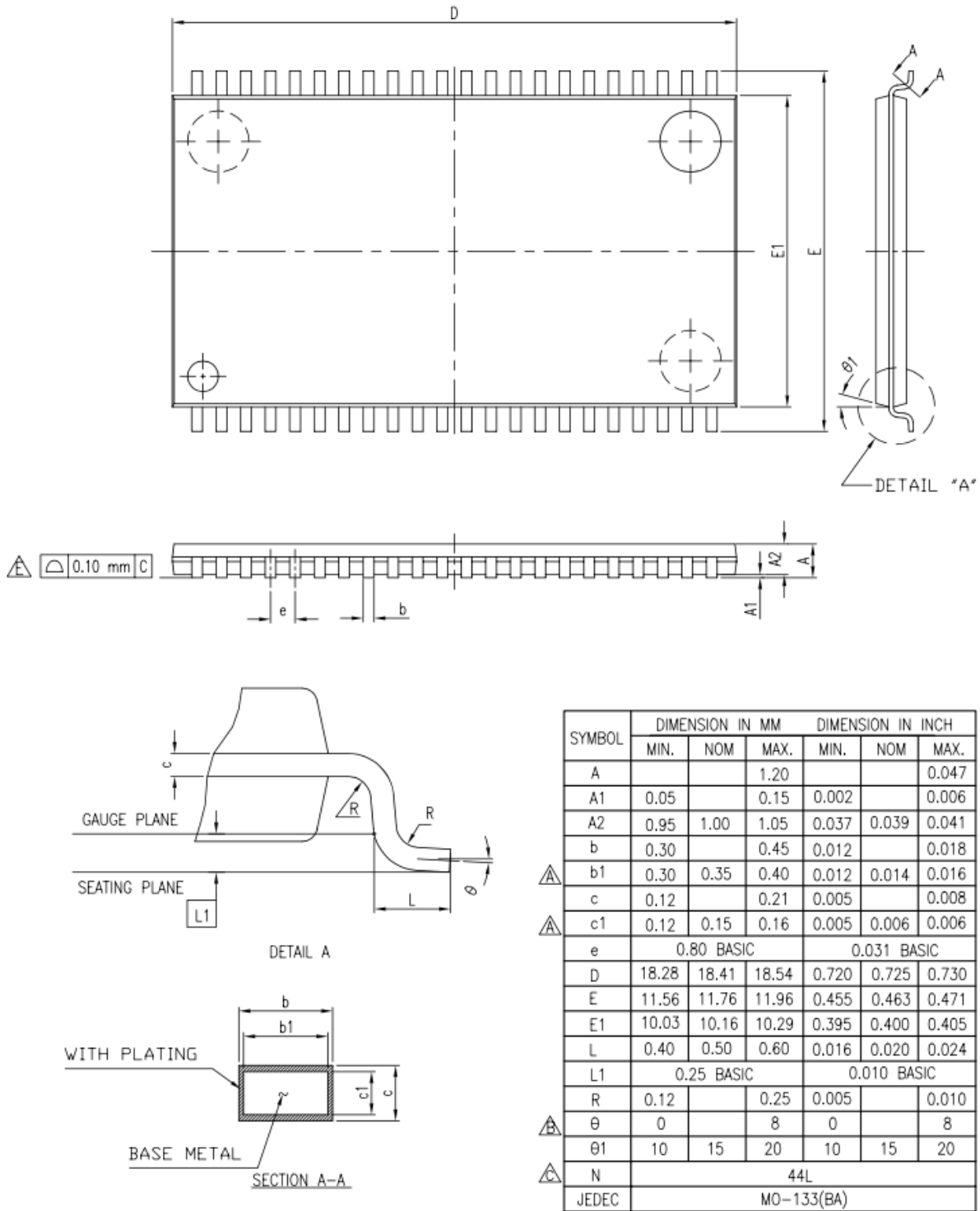
### 48-Ball FBGA (4-32Mb) (Balls Down, Top View)





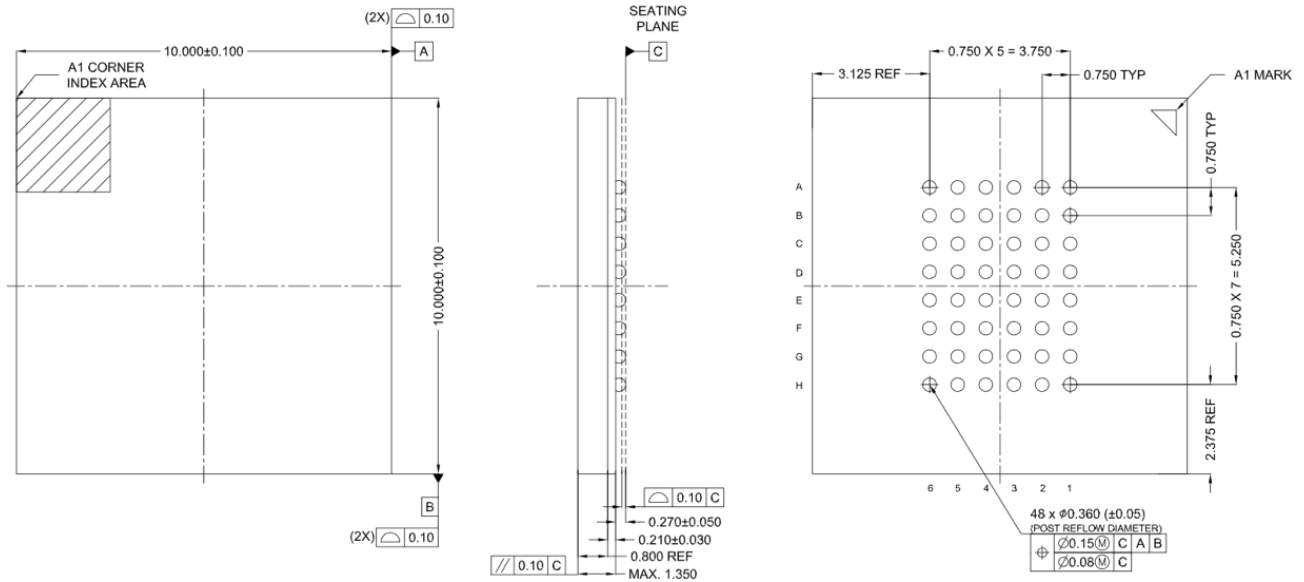
# Package Drawings

## 44-Pin TSOP



NOTE : DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSIONS.  
 D AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

## 48-Ball FBGA



(Unit : mm)

		COMMON DIMENSIONS		
		MIN	NOM	MAX
Package		48 FBGA		
Body size	X	9.900	10.000	10.100
	Y	9.900	10.000	10.100
Ball Pitch		0.750		
Total Thickness		1.350		
Mold Thickness		0.800 Ref.		
Substrate Thickness		0.180	0.210	0.240
Ball Diameter (Raw Ball Size)		0.350		
Stand Off		0.220	0.270	0.320
Ball Width (Post Reflow size)		0.310	0.360	0.410
Package Edge Tolerance		0.100		
Mold Parallelism		0.100		
Coplanarity		0.100		
Ball Offset (Package)		0.150		
Ball Offset (Ball)		0.050		
Ball Count		63		
Edge Ball Center to Center	X	3.750		
	Y	5.250		

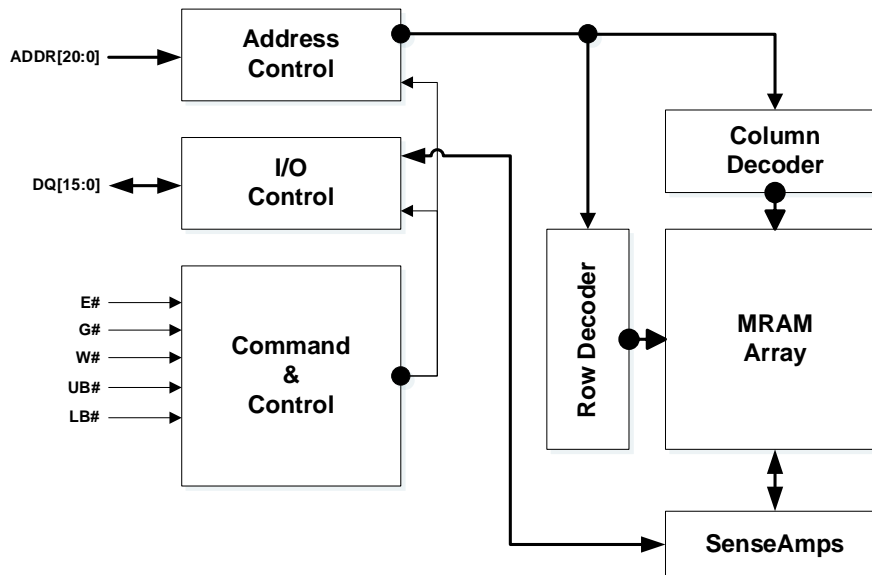
## Architecture

AS3xxx316 is a high performance MRAM device. Writing to and reading from the device as follows:

To write to the device, bring Chip Enable (E#) and Write Enable (W#) inputs Low (Logic '0'). This enables data on I/O pins (DQ[0] to DQ[15]) to be written into the memory location specified by the address pins ADDR[0] through ADDR[20] (48-ball FBGA) and ADDR[0] through ADDR[17] (44-pin TSOP).

To read from the device, bring Chip Enable (E#) input Low (Logic '0'), Output Enable (G#) input Low (Logic '0') while maintaining Write Enable (W#) High (Logic '1'). This enables data from the memory location specified by the address pins ADDR[0] through ADDR[20] (48-ball FBGA) and ADDR[0] through ADDR[17] (44-pin TSOP) to appear on I/O pins (DQ[0] to DQ[15]).

**Figure 3: Functional Block Diagram**



**Table 4: Modes of Operation**

Mode	E#	G#	W#	UB# <sup>1</sup>	LB#	Current	DQ[15:8]	DQ[7:0]
Not Selected	H	X	X	X	X	I <sub>SB</sub>	Hi-Z	Hi-Z
Output Disabled	L	H	H	X	X	I <sub>READ</sub>	Hi-Z	Hi-Z
Output Disabled	L	X	X	H	H	I <sub>READ</sub>	Hi-Z	Hi-Z
Read Upper Byte	L	L	H	L	H	I <sub>READ</sub>	Dataout	Hi-Z
Read Lower Byte	L	L	H	H	L	I <sub>READ</sub>	Hi-Z	Dataout
Read Word	L	L	H	L	L	I <sub>READ</sub>	Dataout	Dataout
Write Upper Byte	L	X	L	L	H	I <sub>WRITE</sub>	Datain	Hi-Z
Write Lower Byte	L	X	L	H	L	I <sub>WRITE</sub>	Hi-Z	Datain
Write Word	L	X	L	L	L	I <sub>WRITE</sub>	Datain	Datain

**Notes:**

H: High (Logic '1')

L: Low (Logic '0')

X: Don't Care

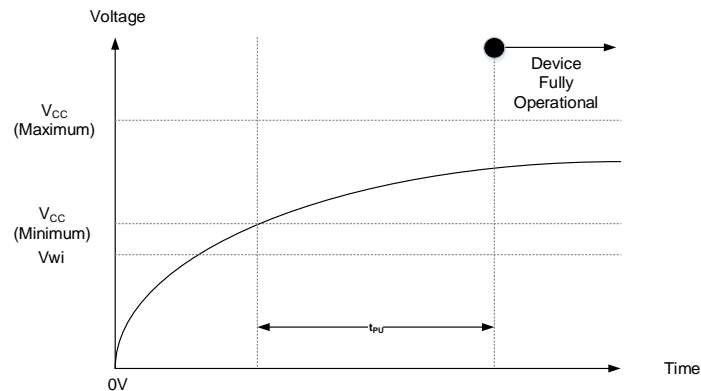
Hi-Z: High Impedance

## Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- E#, W#, G# must follow  $V_{CC}$  during power-up

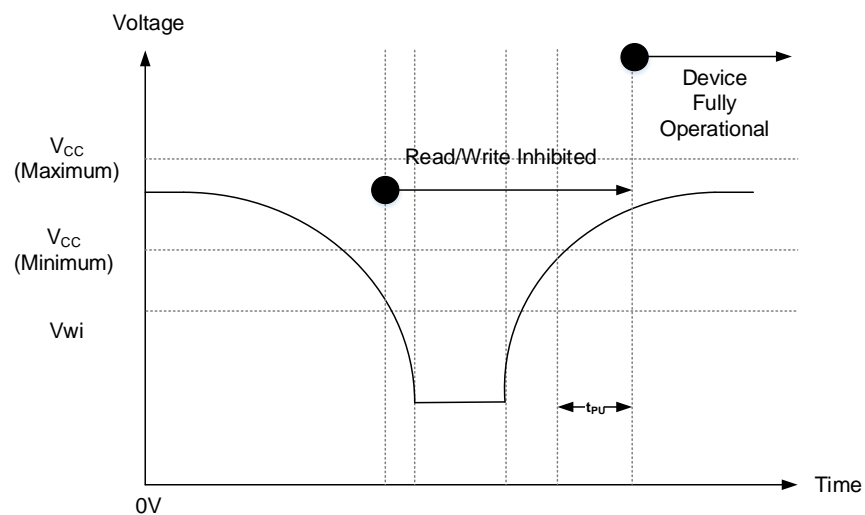
**Figure 4: Power-Up Behavior**



When powering down, the following procedure is required to turn off the device correctly:

- E#, W#, G# must follow  $V_{CC}$  during power-down
- During power loss or brownout, where  $V_{cc}$  goes below  $V_{wi}$ , read/write operations are prohibited. The power-up timing needs to be observed after  $V_{cc}$  goes above  $V_{cc}$  (minimum)

**Figure 5: Power-Down Behavior**



**Table 6: Device Initialization Timing – 3.0V**

Parameter	Symbol	Test Conditions	3.0V			Units
			Minimum	Typical	Maximum	
<b>V<sub>CC</sub> Range</b>		All operating voltages and temperatures	2.7	-	3.6	V
<b>V<sub>CC</sub> Power Up to First Instruction</b>	t <sub>PU</sub>	All operating voltages and temperatures	1	-	-	ms

## Electrical Specifications

**Table 7: Recommended Operating Conditions**

Parameter / Condition		Minimum	Typical	Maximum	Units
	Industrial	-40.0	-	85.0	°C
	Industrial Plus	-40.0	-	105.0	°C
<b>V<sub>CC</sub> Supply Voltage</b>	3.0V	2.7	3.0	3.6	V
<b>V<sub>SS</sub> Supply Voltage</b>		0.0	0.0	0.0	V
<b>V<sub>wi</sub> Write Inhibit Voltage</b>		2.1	2.3	2.5	V

**Table 8: Pin Capacitance**

Parameter	Test Conditions	Symbol	Maximum	Units
<b>Input Pin Capacitance</b>	TEMP = 25°C; f = 1 MHz; V <sub>IN</sub> = 0V Density = 4Mb – 16Mb	C <sub>IN</sub>	10.0	pF
	TEMP = 25°C; f = 1 MHz; V <sub>IN</sub> = 0V Density = 32Mb		20.0	
<b>Input / Output Pin Capacitance</b>	TEMP = 25°C; f = 1 MHz; V <sub>IN</sub> = 0V Density = 4Mb – 16Mb	C <sub>INOUT</sub>	10.0	pF
	TEMP = 25°C; f = 1 MHz; V <sub>IN</sub> = 0V Density = 32Mb		20.0	

**Table 9: DC Characteristics**

Parameter	Symbol	Test Conditions	3.0V Device (2.7V-3.6V)			Units	
			Minimum	Typical	Maximum		
Read Current	I <sub>READ</sub>	V <sub>CC</sub> (max), I <sub>OUT</sub> =0mA	4Mb – 32Mb	-	12.0	30.0	mA
Write Current	I <sub>WRITE</sub>	V <sub>CC</sub> (max)	4Mb – 32Mb	-	20.0	30.0	mA
Standby Current Industrial (-40°C to 85°C)	I <sub>SB</sub>	E#=V <sub>IH</sub> , V <sub>CC</sub> (max)	4Mb-16Mb	-	1.5	2.5	mA
			32Mb		3.0	5.0	
Standby Current Industrial Extended (-40°C to 105°C)	I <sub>SB</sub>	E#=V <sub>IH</sub> , V <sub>CC</sub> (max)	4Mb-16Mb	-	1.7	3.5	mA
			32Mb		3.4	7.0	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =0 to V <sub>CC</sub> (max)		-	-	±1.0	µA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> =0 to V <sub>CC</sub> (max)		-	-	±1.0	µA
Input High Voltage	V <sub>IH</sub>			0.8xV <sub>CC</sub>	-	V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>			-0.5	-	0.2xV <sub>CC</sub>	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> = -1.6mA		V <sub>CC</sub> -0.5	-	-	V
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA		-	-	0.4	V

**Table 10: Magnetic Immunity Characteristics**

Parameter	Symbol	Maximum	Units
Magnetic Field During Write	H <sub>max_write</sub>	24000	A/m
Magnetic Field During Read	H <sub>max_read</sub>	24000	A/m

**Table 11: AC Test Conditions**

<b>Parameter</b>	<b>Value</b>
<b>Input pulse levels</b>	0.0V to $V_{CC}$
<b>Input rise and fall times</b>	5ns
<b>Input and output measurement timing levels</b>	$V_{CC}/2$
<b>Output Load</b>	CL = 30pF



## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. Exposure to maximum rating for extended periods may adversely affect reliability.

**Table12: Absolute Maximum Ratings**

Parameter	Minimum	Maximum	Units
Magnetic Field During Write	---	24000	A/m
Magnetic Field During Read	---	24000	A/m
Junction Temperature	---	125	°C
Storage Temperature	-55 to 150		°C
Supply Voltage Vcc relative to Vss	-0.5	4.0	V
Voltage on any pin	-0.5	Vcc + 0.4	V
DC output current Iout	± 20		mA
ESD HBM (Human Body Model) ANSI/ESDA/JEDEC JS-001-2017	≥  2000 V		V
ESD CDM (Charged Device Model) ANSI/ESDA/JEDEC JS-002-2018	≥  500 V		V
Latch-Up (I-test) JESD78	≥  100 mA		mA
Latch-Up (Vsupply over-voltage test) JESD78	Passed		---

## Write Operation

Figure 7: Write Operation (W# Controlled)

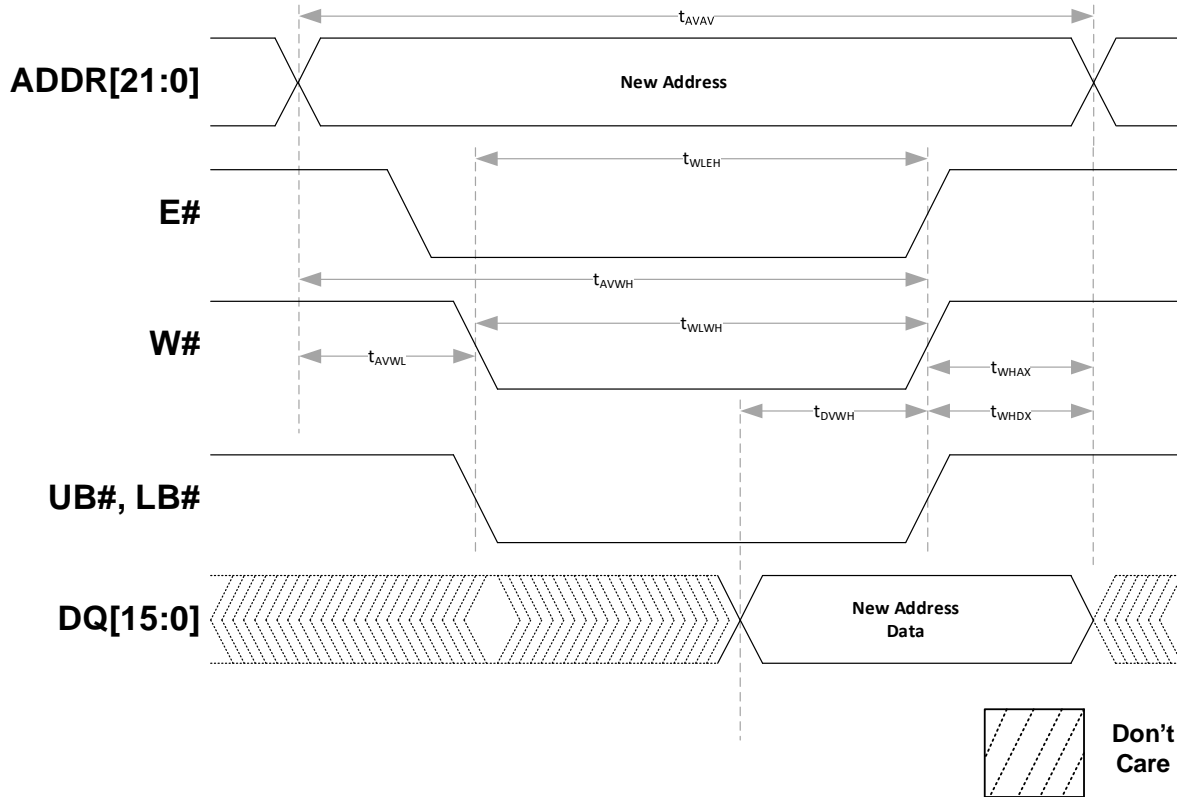


Table 13: Write Operation (W# Controlled)

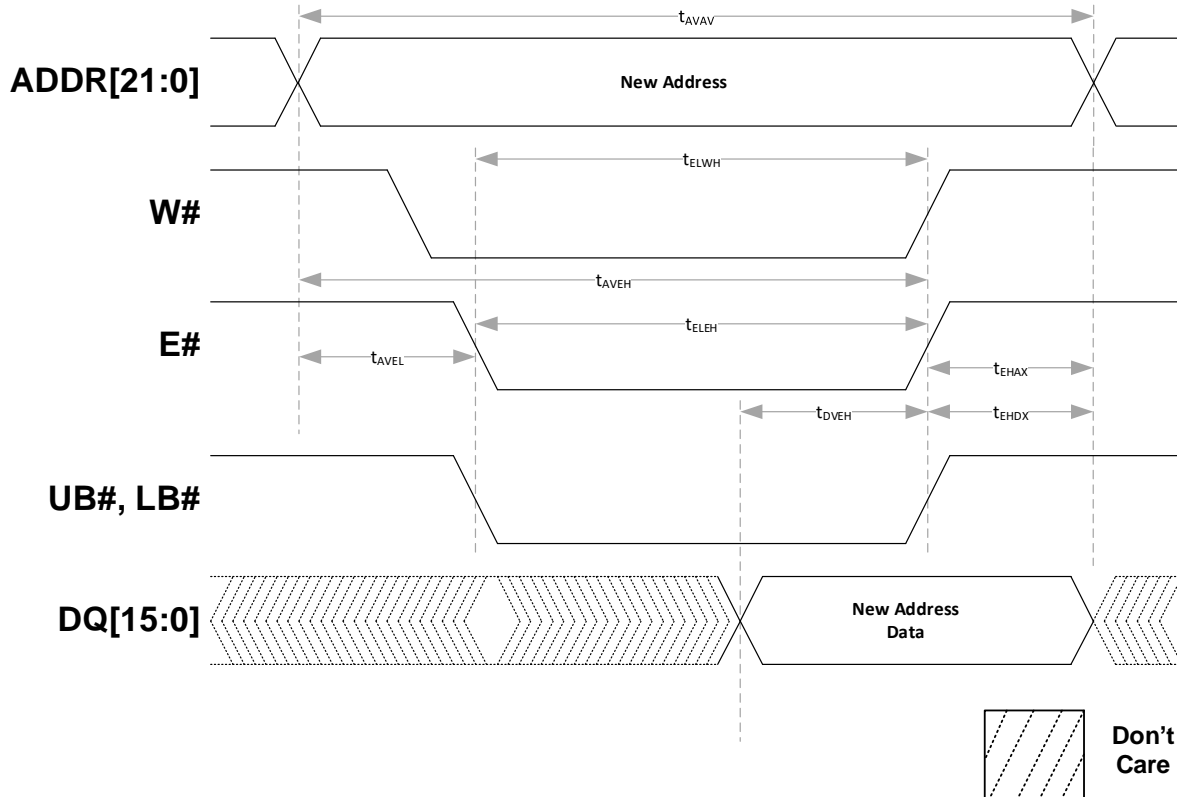
Parameter	Symbol	Minimum		Maximum	Units
		35ns	45ns		
Write Cycle Time	$t_{AVAV}$	35	45	-	ns
Address Set-Up Time	$t_{AVWL}$	0		-	ns
Address Valid to end of Write (G# High)	$t_{AVWH}$	18	28	-	ns
Address Valid to end of Write (G# Low)	$t_{AVWH}$	20	30	-	ns
Write Pulse Width (G# High)	$t_{WLWH}, t_{WLEH}$	15	25	-	ns
Write Pulse Width (G# Low)	$t_{WLWH}, t_{WLEH}$	15	25	-	ns
Data Valid to end of Write	$t_{DVWH}$	10	15	-	ns
Data Hold Time	$t_{WHDX}$	0		-	ns
Write recovery Time	$t_{WHAX}$	12		-	ns

**Notes:**

G# is High (Logic '1') for Write operation

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

**Figure 8: Write Operation (E# Controlled)**

**Table 14: Write Operation (E# Controlled)**

Parameter	Symbol	Minimum		Maximum	Units
		35ns	45ns		
Write Cycle Time	$t_{AVAV}$	35	45	-	ns
Address Set-Up Time	$t_{AVEL}$	0		-	ns
Address Valid to end of Write (G# High)	$t_{AVEH}$	18	28	-	ns
Address Valid to end of Write (G# Low)	$t_{AVEH}$	20	30	-	ns
Write Pulse Width (G# High)	$t_{ELWH}, t_{ELEH}$	15	25	-	ns
Write Pulse Width (G# Low)	$t_{ELWH}, t_{ELEH}$	15	25	-	ns
Data Valid to end of Write	$t_{DVEH}$	10	15	-	ns
Data Hold Time	$t_{EHDX}$	0		-	ns
Write recovery Time	$t_{EHAX}$	12		-	ns

**Notes:**

G# is High (Logic '1') for Write operation

Power supplies must be stable

Addresses valid either before or at the same time as W# goes low

## Bus Turnaround Operation – Read to Write

Figure 9: Bus Turnaround Operation

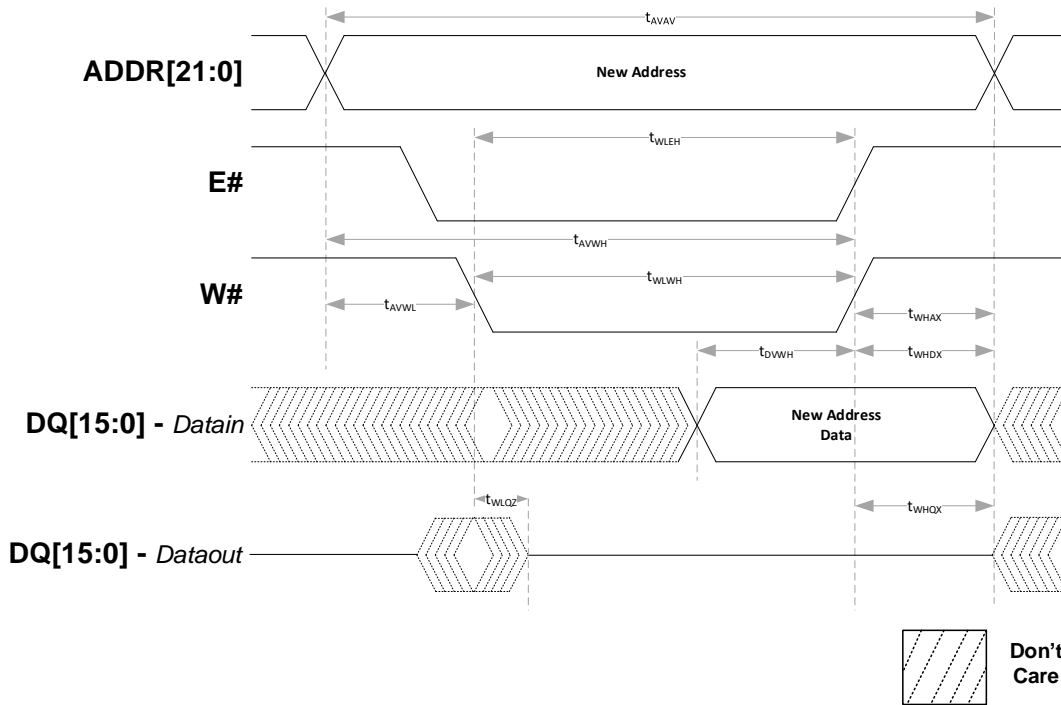


Table 15: Bus Turnaround

Parameter	Symbol	Minimum	Maximum		Units
			35ns	45ns	
<b>W# Low to Data Hi-Z</b>	$t_{WLQZ}$	0	12	15	ns
<b>W# High to Output Active</b>	$t_{WHQX}$	3	-		ns

**Notes:**

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

## Read Operation

Figure 10: Read Operation

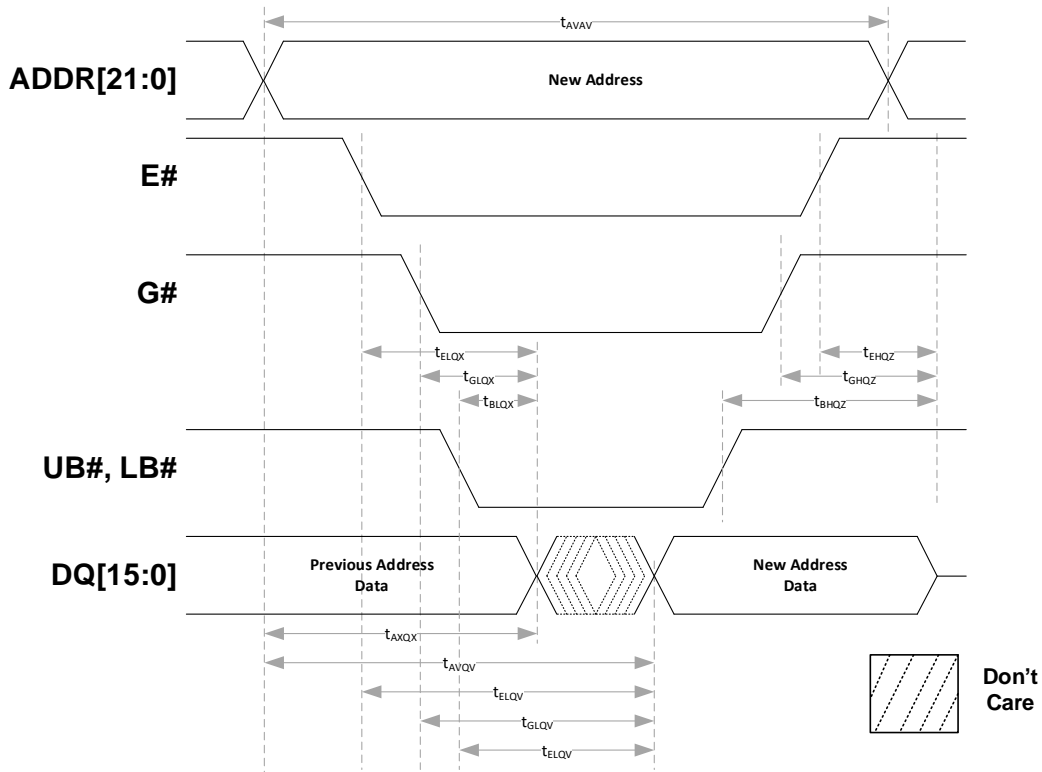


Table 16: Read Operation

Parameter	Symbol	Minimum		Maximum		Units
		35ns	45ns	35ns	45ns	
Read Cycle Time	$t_{AVAV}$	35	45	-		ns
Address Cycle Time	$t_{AVQV}$	-		35	45	ns
Chip Enable Access Time	$t_{ELQV}$	-		35	45	ns
Output Enable Access Time	$t_{GLQV}$	-		15	25	ns
Byte Enable Access Time	$t_{BLQV}$	-		15	25	ns
Output Hold From Address Change	$t_{AXQX}$	3		-		ns
Chip Enable Low to Output Active	$t_{ELQX}$	3		-		ns
Output Enable Low to Output Active	$t_{GLQX}$	0		-		ns
Byte Enable Low to Output Active	$t_{BLQX}$	0		-		ns
Chip Enable High to Output Hi-Z	$t_{EHQZ}$	0			15	ns
Output Enable High to Output Hi-Z	$t_{GHQZ}$	0		10	15	ns
Byte Enable High to Output Hi-Z	$t_{BHQZ}$	0			10	ns

**Notes:**

W# is High (Logic '1') for Read operation

Power supplies must be stable

Addresses valid either before or at the same time as E# goes low

## Endurance and Data Retention

*Table 17: Endurance and Data Retention*

Parameter	Symbol	Test Conditions	Minimum	Units
<b>Write Endurance</b>	END	-	10 <sup>14</sup>	cycles
<b>Data Retention</b>	RET	105°C	10	years
		85°C	1,000	
		75°C	10,000	
		65°C	1,000,000	

## Thermal Resistance

**Table 18: Thermal Resistance Specifications**

Parameter	Description	Test Conditions	44-pin TSOP (4Mb)	48 Ball FBGA (4Mb - 16Mb)	48 Ball FBGA (32Mb)	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	40.05	42.67	43.98	°C/W
$\theta_{JC}$	Thermal resistance (junction to case)		7.02	11.09	11.82	

**Notes:**

1: These parameters are guaranteed by characterization; not tested in production.

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## Revision History

Revision	Date	Change Summary
<b>REV Q</b>	12/01/2020	Updated Package Drawings – 44-Pin TSOP, 54-Pin TSOP and 48-Ball FBGA Removed “Preliminary” from the footer. Added REACH Compliance
<b>REV R</b>	07/16/2021	Updated max values for I <sub>READ</sub> , I <sub>SB</sub> , I <sub>SLP</sub> in Table 9 (DC Characteristics). Removed Sleep mode SE# functionality. This function has been removed to be 100% functionally compatible with legacy devices. The previously assigned Pin or Ball is now designated as “NC”. Updated Product Use Limitations.
<b>REV S</b>	8/24/2021	Added 64Mb density. Updated max values for I <sub>READ</sub> , I <sub>SB</sub> , I <sub>SLP</sub> in Table 9 (DC Characteristics)
<b>REV T</b>	4/18/2022 5/09/2022 5/18/2022	Added Absolute Maximum Ratings Table Corrected Table 6 : V <sub>CC</sub> Power Up to First Instruction = 1ms Fixed a spelling mistake
<b>REV U</b>	07/30/2024	Removed 1Mb, 64Mb density options Removed TSOP 54 Package option Removed Tape and Reel Packing option