Gen 3 Space Grade Serial Dual QSPI 64Mb-128Mb P-SRAM™ Development Kit User Guide AK30X208LATCTSOE

Table 1: Revision History

Revision No.	Date	History
1.0	08/21/2024	Initial Release

Contents

1. Overview

The Avalanche Gen 3 Space Serial Dual QSPI 64Mb-128Mb P-SRAM™ development kit enables the users to evaluate Avalanche Serial Dual QSPI 64Mb-128Mb P-SRAM™ product using a Lattice LCMXO3L/LF-6900C FPGA Development Kit connected to Avalanche socketed daughter board via Avalanche proprietary FPGA based Asynchronous SRAM interface. The Gen 3 Space Serial Dual QSPI 64Mb-128Mb P-SRAM™ development kit communicates with the computer via USB interface using a micro-USB cables type B connector.

2. Development Kit Ordering Info

Table 1: Development Kit Socketed Ordering Info

Part #	Description
AK30X208LATCTSOE	**Gen 3 Dual QSPI 64Mb-128Mb Standard Kit** – 56-Ball FBGA socketed daughter board (for MRAM*) with Lattice FPGA board

Note: * MRAM devices orderable separately

3. Ordering Options

3.1 Development Kit

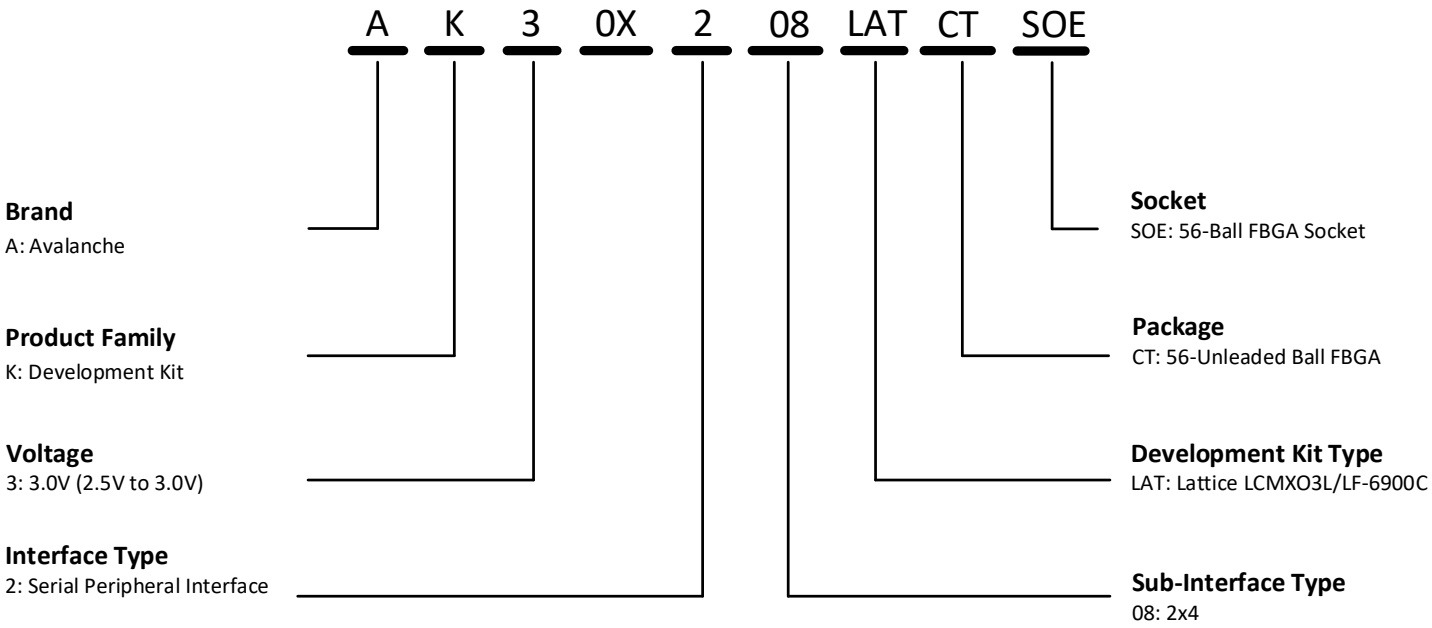


Figure 1: Development Kit Ordering Information

3.2 56-Ball FBGA Socket

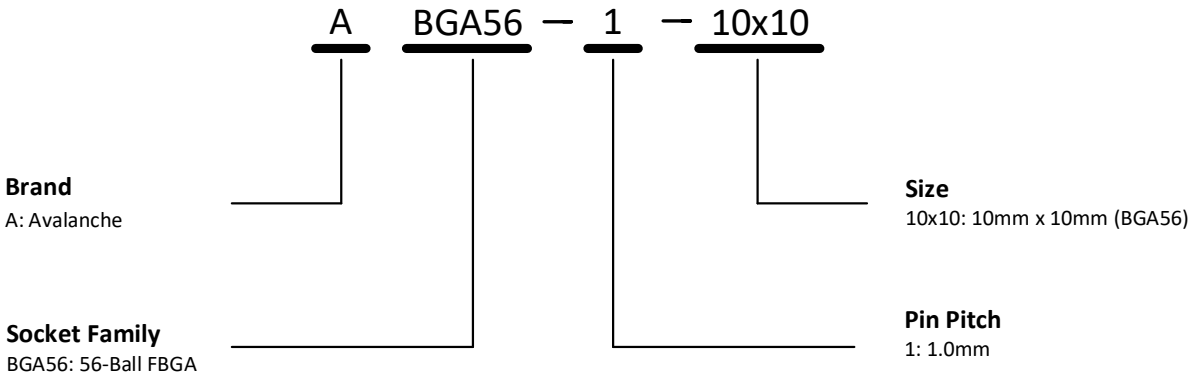


Figure 2: 56-Ball FBGA Socket Ordering Information

4. Development Kit Package Contents

1. An Avalanche daughter board (3.5 x 3.5 inches) with a 56-Ball FBGA socket
2. A Lattice LCMXO3L/LF-6900C FPGA board
3. A micro-USB cable type B
4. A 3.3V 2A AC/DC power supply cord

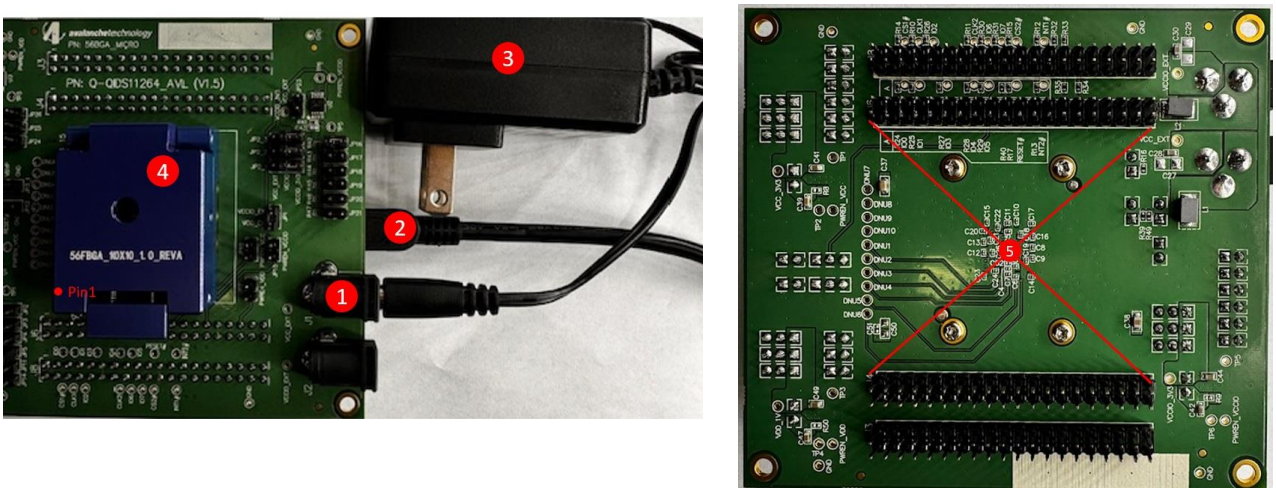


Figure 3: Serial Dual QSPI P-SRAM™ Daughter Board with a 56-Ball FBGA Socket (Front & Back)

Table 2: Development Kit Setup Description

Callout Number	Description
1	J1 Power Barrel Connector Jack*
2	USB type Mini-B cable connecting from Lattice LCMXO3L/LF-6900C FPGA board to PC host
3	3.3V 2A AC/DC power supply cord
4	Avalanche 56-Ball FBGA socket
5	4 double-row Arduino male headers connecting to Lattice LCMXO3L/LF-6900C FPGA board

*Note: *Plug polarity on the Power Barrel Connector Jack: P = Center Positive*

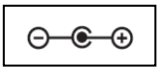


Table 3: Jumper Settings

Function	Jumper #	Description	Default Setting
Power Supply Selection	**JP1**	**ON = Single 3.3V External Power Supply Enabled**	**ON**
Lattice Vccio Enable	**JP6**	**ON = Supplying Lattice Vccio from External Power Source**	**ON**
Vcc Regulator Enable	**JP1_1**	**ON = 1-2 Enabling Vcc Regulator**	**1-2**
	JP1_2		**1-2**
	JP1_3		**1-2**
Vccio Regulator Enable	**JP2_1**	**ON = 1-2 Enabling Vccio Regulator**	**1-2**
	JP2_2		**1-2**
	JP2_3		**1-2**
Vcc Selection	JP2	Reserved	OFF
	JP3	Reserved	OFF
	JP4	**ON = 3.0V (Vcc)**	**ON**
	JP5	Reserved	OFF
	JP11	ON = 2.5V (Vcc)	OFF
	JP14	Reserved	OFF
Vccio Selection	**JP16**	**ON = 1.8V (Vccio)**	**ON**
	JP17	ON = 2.5V (Vccio)	OFF
	JP18	ON = 3.0V (Vccio)	OFF
	JP19	ON = 3.3V (Vccio)	OFF
	JP20	Reserved	OFF
	JP21	Reserved	OFF

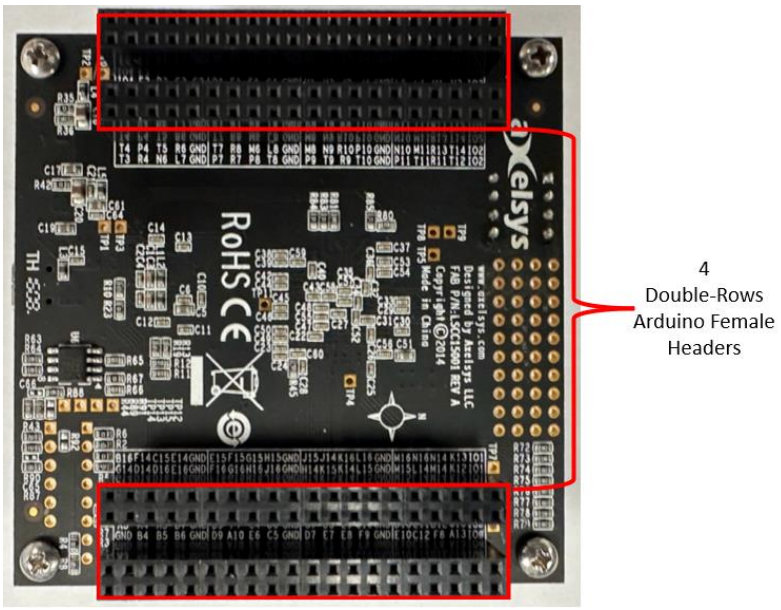


Figure 4: Lattice LCMXO3L/LF-6900 FPGA board (back side) with 4 Double-Rows Arduino Female Headers

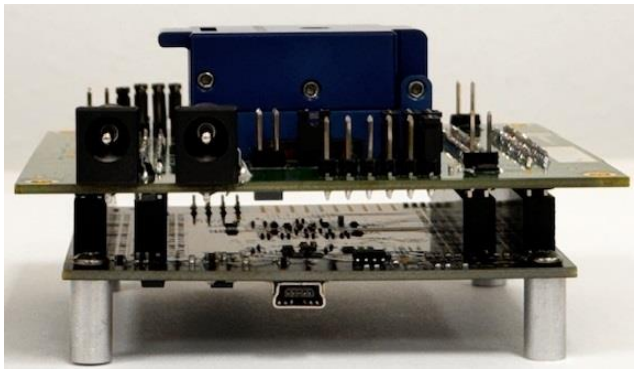


Figure 5: Serial Dual QSPI 64Mb-128Mb P-SRAM™ Daughter Board Attaching to Lattice Board

Note: a Lattice LCMXO3L/LF board requires to have 4 double-rows of Arduino female headers installed to connect it to the Avalanche daughter board.

5. Getting Started

The following steps are necessary to operate the kit.

5.1 Requirements

- A PC system with one available USB 2.0/3.0 port
- Windows 10 with 32/64-bit Operation System
- FTDI USB Window drivers

- Avalanche application software
- Avalanche Serial Dual QSPI P-SRAM Development Kit

5.2 FTDI USB Drivers Installations

Communication between the Lattice LCMXO3 board and a PC via the USB connection cable requires installation of the FTDI USB hardware drivers. Loading these drivers enables the PC to recognize the Lattice board. Click here to download the drivers.

Note: first install the FTDI drivers and then connect the Lattice LCMXO3 board to the PC

5.3 Avalanche Application Software

Click here to download the software package in zip format.

5.4 Configuring Vcc and Vccio and Connecting the Development Kit to the PC

Perform the step-by-step instructions in the following order to configure and connect the Development Kit to the PC:

1. Select Vcc jumper on the board (Default JP4 = ON = 3.0V)
2. Select Vccio jumper on the board (Default JP16 = ON = 1.8V)
    - To ensure the test software is configured correctly at Vccio of 1.8V, set "VCCIO_Sel = 1" in the Config.txt
3. Plug a center-positive plug into the board's **J1** power jack
4. Connect the 3.3V 2A power supply cord to power outlet
5. Turn on the Lattice board by connecting the Lattice LCMXO3 to the PC using the USB Mini-B cable. The PURPLE power LEDs on the Lattice board should stay on after connection.

5.5 Running Avalanche Test Program

The Lattice LCMXO3 board is pre-loaded with proprietary Avalanche FPGA bitfile and an executable test program. To run the Avalanche test software, double click on "DQSPI_test_menu_cv.exe"

The configuration file consists of six parameters. Below is an example of a config.txt file:

- Def_port = 1
    - Use "1" as the default COM port.
- Run_test = y/n
    - y: automated test. The test starts automatically once the "DQSPI_test_menu_cv.exe" is invoked.
    - n: user selected option test. The user can start the test manually.

- Test _selection = g (reserved)
- TPS_Sel_def = 0 (reserved)
- Test_sel = user (reserved)
- Vccio_sel = 1 (Vccio = 1.8V)
    - Vccio voltage can be configured via jumper setting (JP16-JP19 – refer to Table 3 – Jumper Settings)

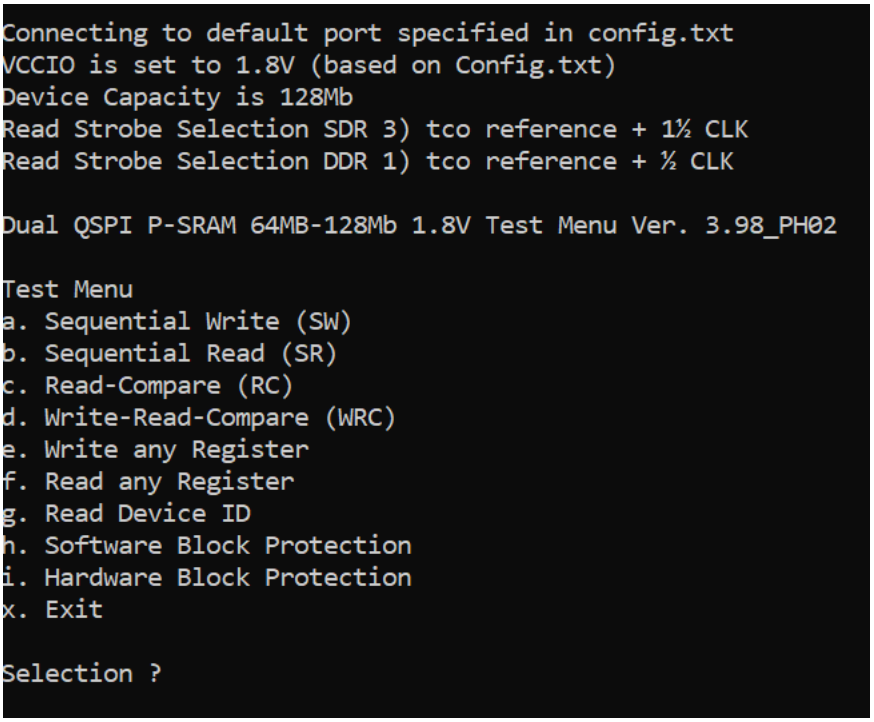


Figure 6: Test Menu

Write Read Compare Test Example – Option d

Step1 – select option d: Write Read Compare (WRC)

Step 2 – enter test profile selection: user can either select a pre-defined test script or manually go to each test input.

Step 3 – enter lane to test: select lane 1 + lane 2 for 128Mb or select lane 1 for 64Mb

A 128Mb Avalanche Serial Dual QSPI P-SRAM connects two Quad SPI devices (P-SRAM 1 & P-SRAM2). Each device has a separate memory address range and can be tested independently. Lane 0 is referenced to P-SRAM 1 (64Mb) and Lane 1 is referenced to P-SRAM 2 (64Mb).

Step 4 – Write-Read-Compare the Entire Capacity (Y/N): select n to test a specific section of the memory array or select y to test the entire memory array.

Step 5 – Enter SDR/DDR Selection: select SDR to test the device in Single Data Rate interface or select DDR to test the device in Double Data Rate.

Step 6 – Enter Starting Address: select starting address in hex format "0x"

Step 7 - Enter Tested Data Size in Bytes up to 0x007fffff: select tested data size in bytes in hex format "0x"

Step 8 - Enter Pattern Type: select tested data pattern type

Step 9 – Data Inverted per Test Loop? (y/n): select y for data pattern to be inverted per test loop (test loop must be greater than 1)

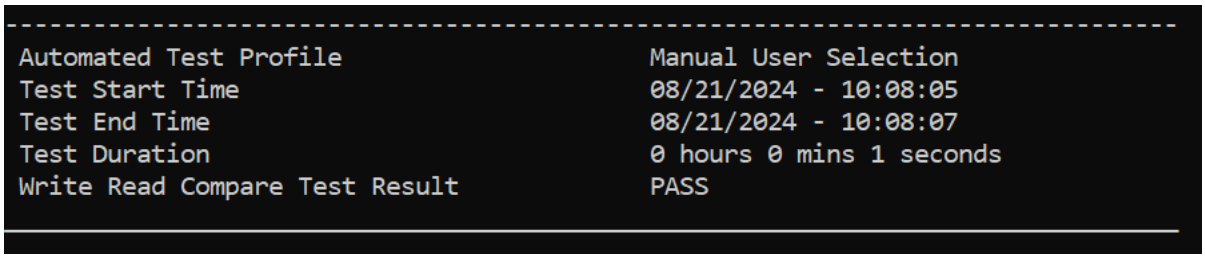
Step 10 - Enter Number of Test Loops (Default = 2):

Step 11 – Stop on Error? (y/n): select y for test to stop on error

Step 12 – Data Log Enable? (y/n): select y for test program to save data log

Step 13 – Print Log Enable? (y/n): select y for test program to display test progress

- Press "Enter" key to start test
- Press "Space" key to pause test
- Press "Esc" key to resume test

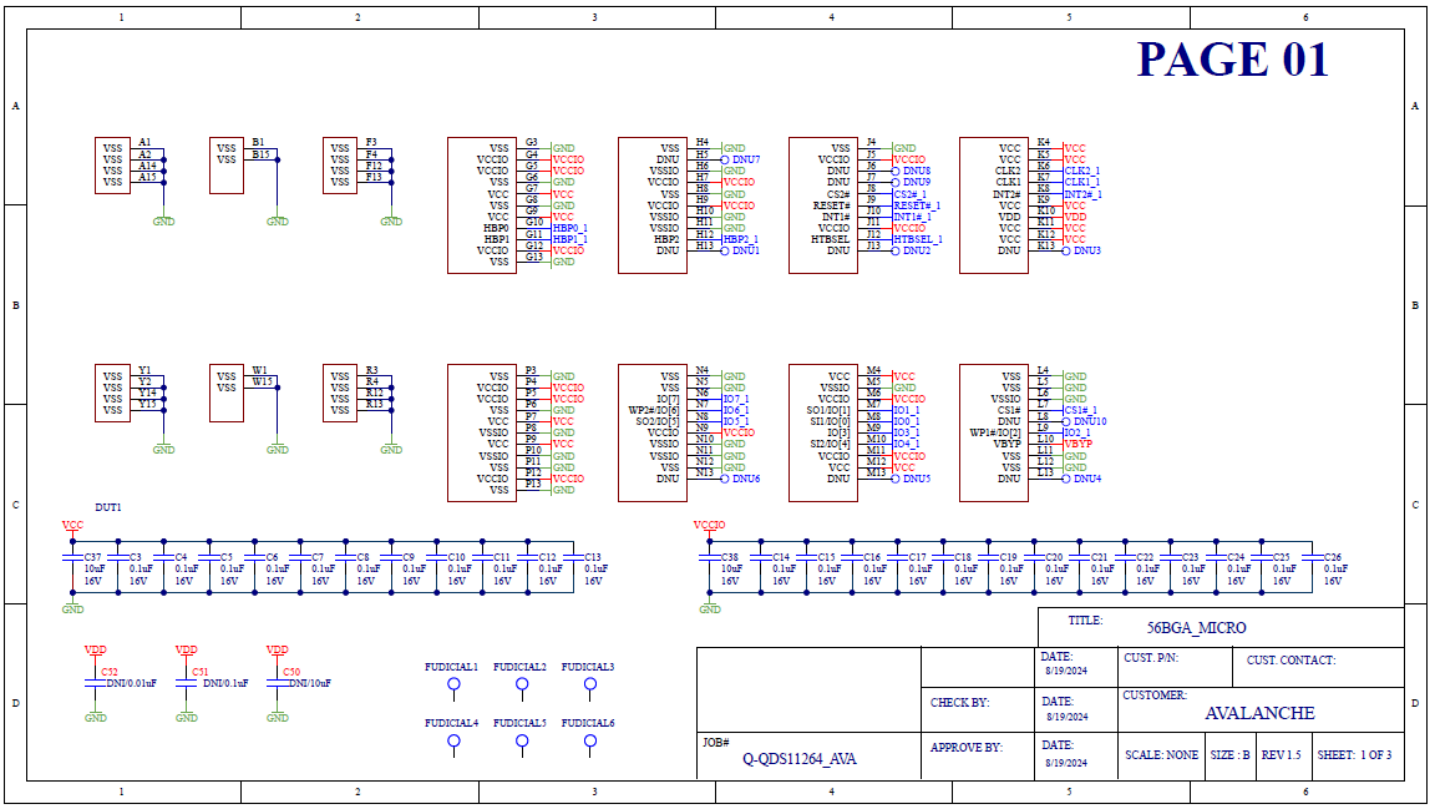


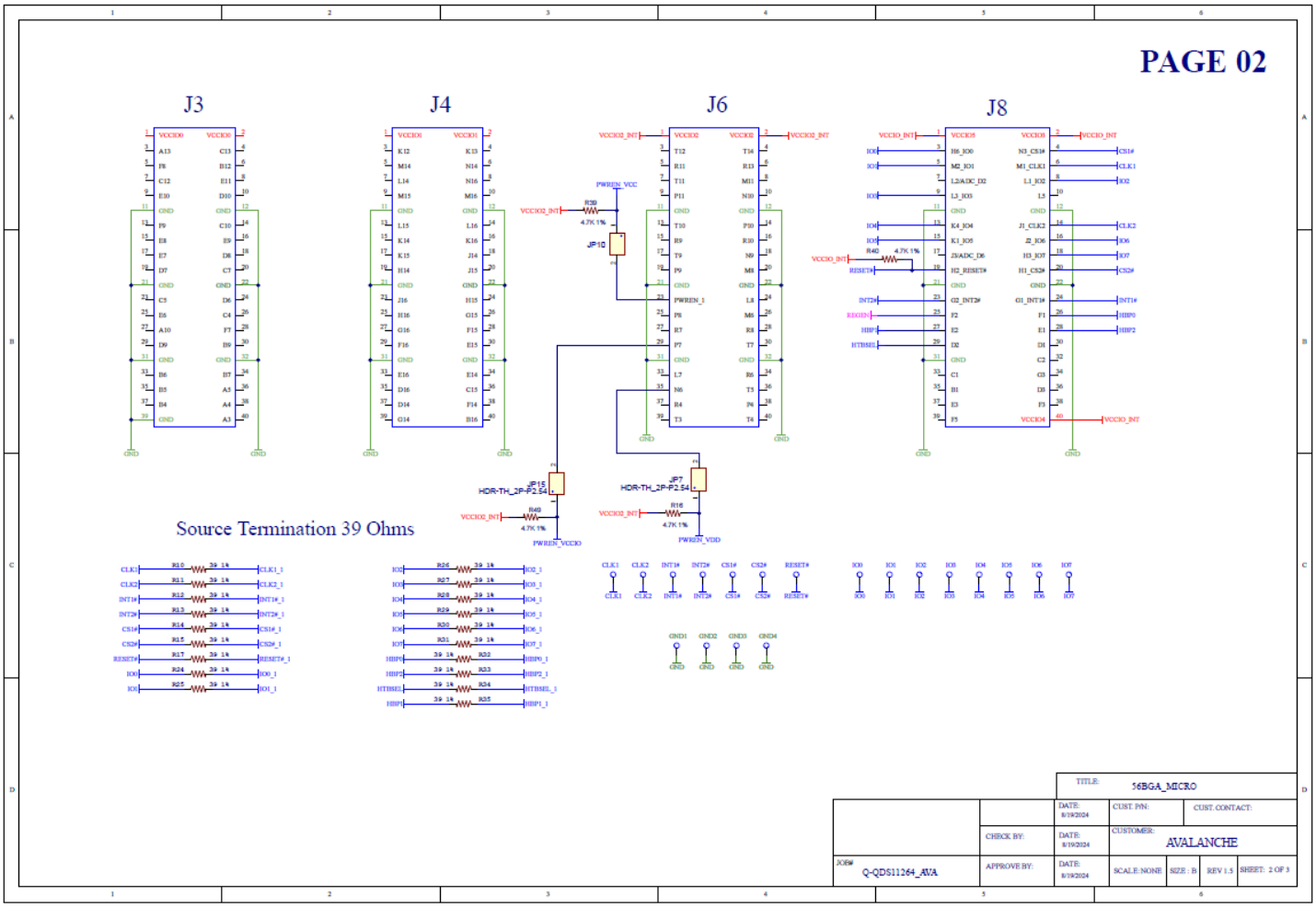
Automated Test Profile	Manual User Selection
Test Start Time	08/21/2024 - 10:08:05
Test End Time	08/21/2024 - 10:08:07
Test Duration	0 hours 0 mins 1 seconds
Write Read Compare Test Result	PASS

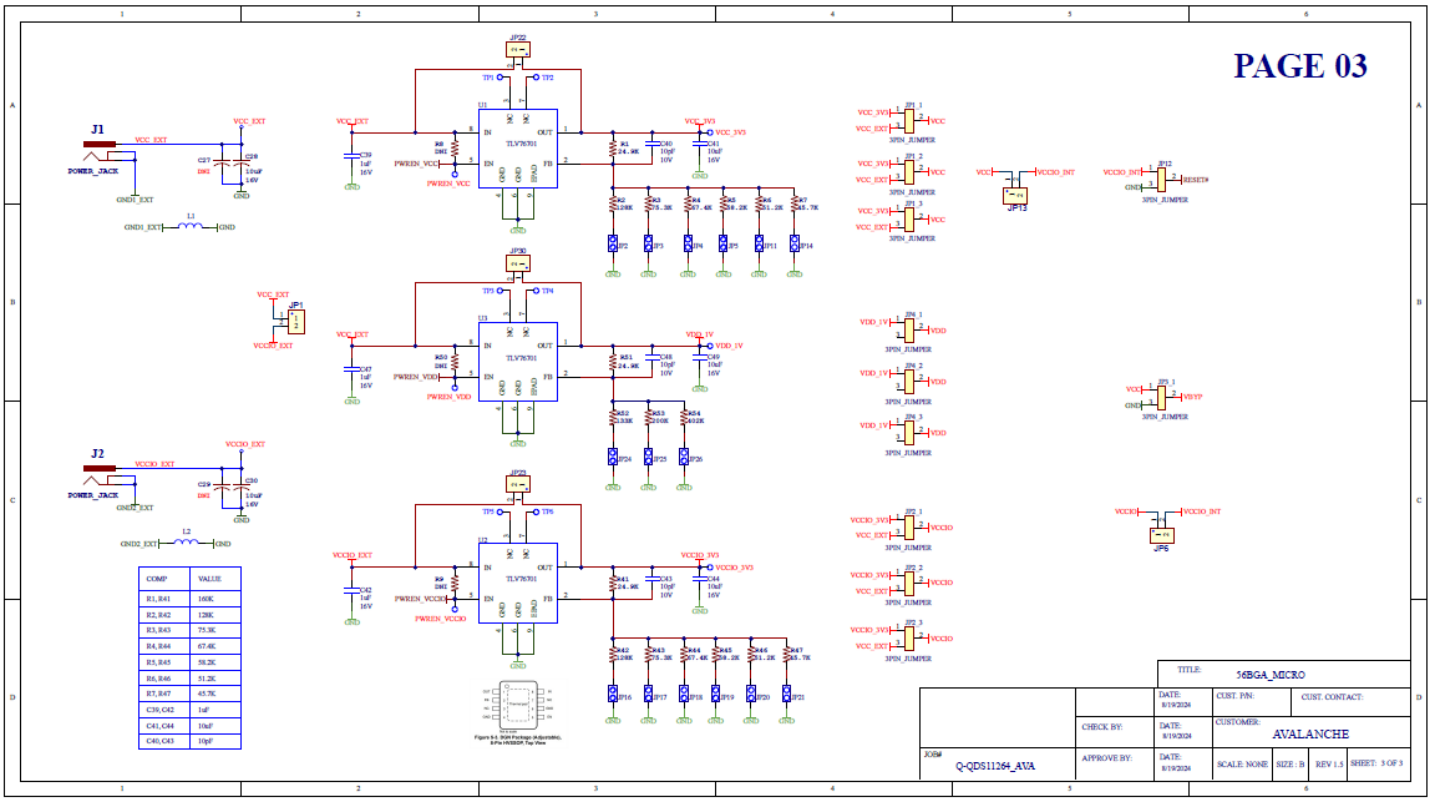
Figure 7: Write Read Compare Test Result Summary

6. Schematics

AK30X208LATCTSOE – Schematic




PAGE 02
J3
J4
J6
J8
Source Termination 39 Ohms
JP15
HDR-TH_2P-P2.54
JP7
HDR-TH_2P-P2.54
JP10
TITLE: 56BGA_MICRO
CUSTOMER: AVALANCHE
JOB# Q-QDS11264_AVA
SCALE:NONE
SIZE : B
REV 1.5
SHEET: 2 OF 3



COMP	VALUE
R1, R41	160K
R2, R42	120K
R3, R43	75.3K
R4, R44	67.4K
R5, R45	59.2K
R6, R46	51.2K
R7, R47	45.7K
C39, C42	1uF
C41, C44	10uF
C40, C43	10pF

7. BOM

AK30X208LATCTSOE – BOM

Qty	Value	Description	Footprint
24	0.1µF	Cap Cer 0.1µ 16V X5R 0201	C0201
2	DNI	DNI	N_1206
5	10 µF	CAP Cer 10 µF 16V X6S 0603	N_0603
2	10 µF	CAP Cer 10 µF 16V X7R 0805	0805C
3	1µF	CAP Cer 1µF 16V X7R 0603	N_0603
3	10 µF	CAP Cer 10µF 10V X7R 0603	N_0603
41	TP	Test Point	Test_Point 40x20 010819
1	DNI/0.01 µF	DNI CAP Cer 10000pF 16V X7R 0402	N_0402
1	DNI/0.1 µF	DNI CAP Cer 0.1µF 16V X7R 0402	N_0402
1	DNI/10 µF	DNI CAP Cer 10µF 16V X7R 0805	N_0805
1	56BGA	BGA	BGA56
6	Fudicial	--	Fudicial
2	Power Jack	Conn PWR Jack 2x5.5mm Solder	Power_Jack_PTH
4	Connector 20POS	Conn Header Vert 20POS 2.54mm	2x10 Header
23	HDR-TH_2P-P2.54	Conn Header Vert 20POS 2.54mm	1x2 Header With Shunt_051914
11	3-Pin Jumper	Conn Header Vert 20POS 2.54mm	Jumper_3Pin
2	2743019447	Ferrite Beads 43 SM Bead Z=47 Ohm @100MHz	FB_2743019447
3	24.9K	Res 24.9K Ohm 1% 1/16W 0402	N_0402
2	128K	Res 127K Ohm 1% 1/16W 0402	N_0402
2	75.3K	Res 75K Ohm 1% 1/16W 0402	N_0402
2	67.4K	Res 67.3K Ohm 1% 1/16W 0402	N_0402
2	58.2K	Res 59K Ohm 1% 1/16W 0402	N_0402
2	51.2K	Res 51.1K Ohm 1% 1/16W 0402	N_0402
2	45.7K	Res 45.3K Ohm 1% 1/16W 0402	N_0402
3	DNI	DNI	N_0402
19	39.1	Res 39Ohm 1% 1/16W 0402	N_0402
3	4.7K	Res 4.7K Ohm 1% 1/16W 0402	N_0402
1	133K	Res 133K Ohm 1% 1/16W 0402	N_0402
1	200K	Res 200K Ohm 1% 1/16W 0402	N_0402

Qty	Value	Description	Footprint
1	402K	Res 402K Ohm 1% 1/16W 0402	N_0402
3	TLV767	Linear Voltage Regulator IC Positive Adjustable 1 Output 1A 8-HVSSOP	TLV767
2	Test Point	Test Point	Test Point