Platforms Enabled by Hi-Rel MRAM

Paul Chopelas, General Manager, Aerospace & Defense
Avalanche Technology

November 5, 2024
RHET Conference
Huntsville, AL

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Agenda

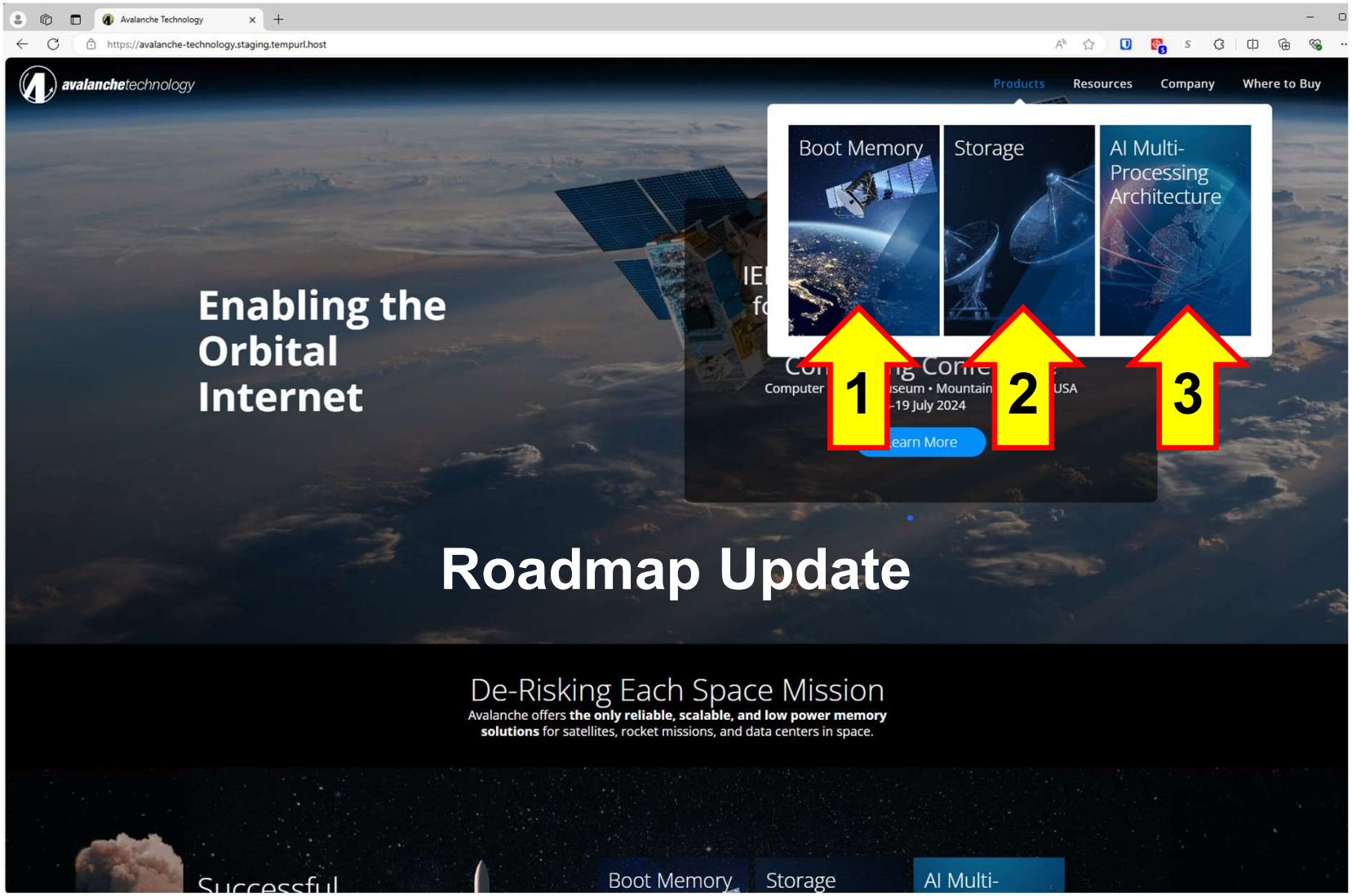
Roadmap, Ecosystem and Radiation Update

Enabled Platforms – Booting

Enabled Platforms – Storage

Enabled Platforms – Processing

Hi-Rel/Space Customers Lallapalooza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Enabling the Orbital Internet
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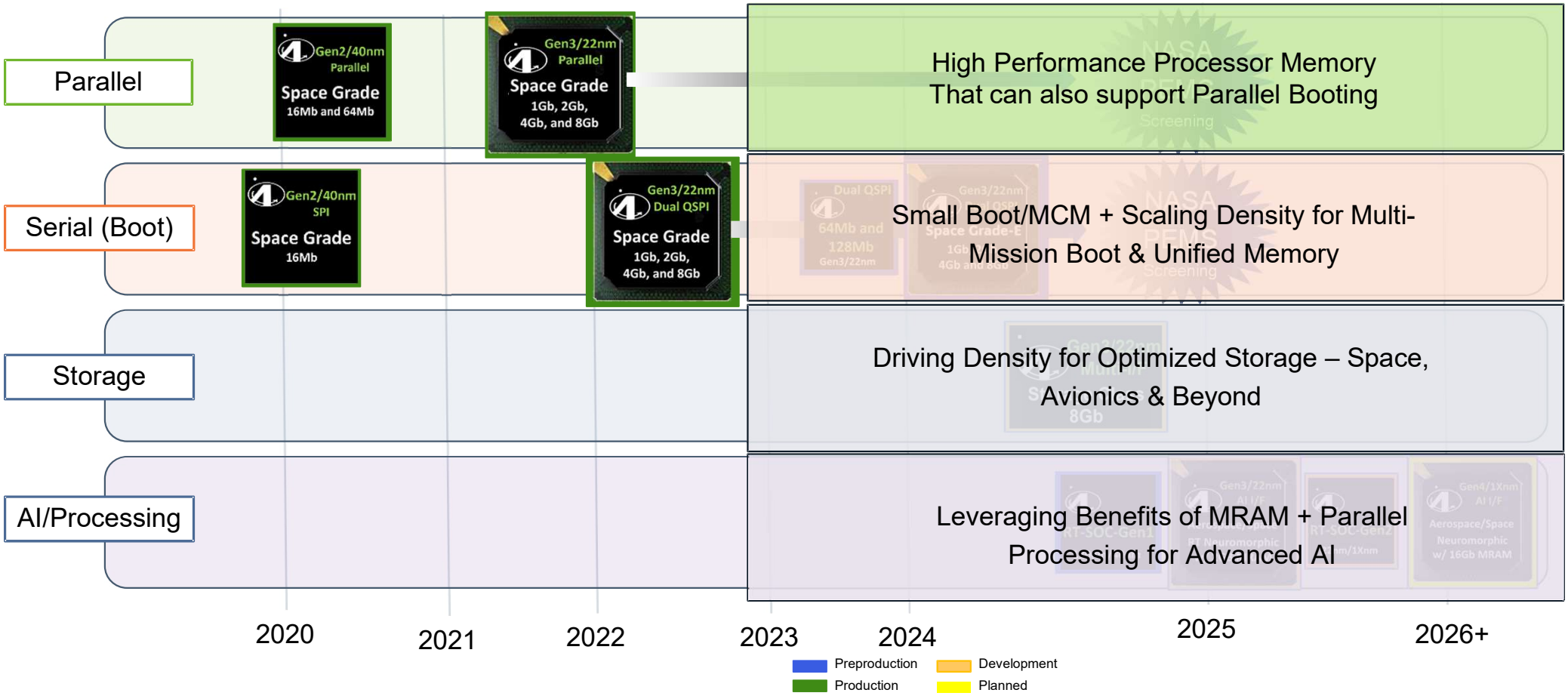
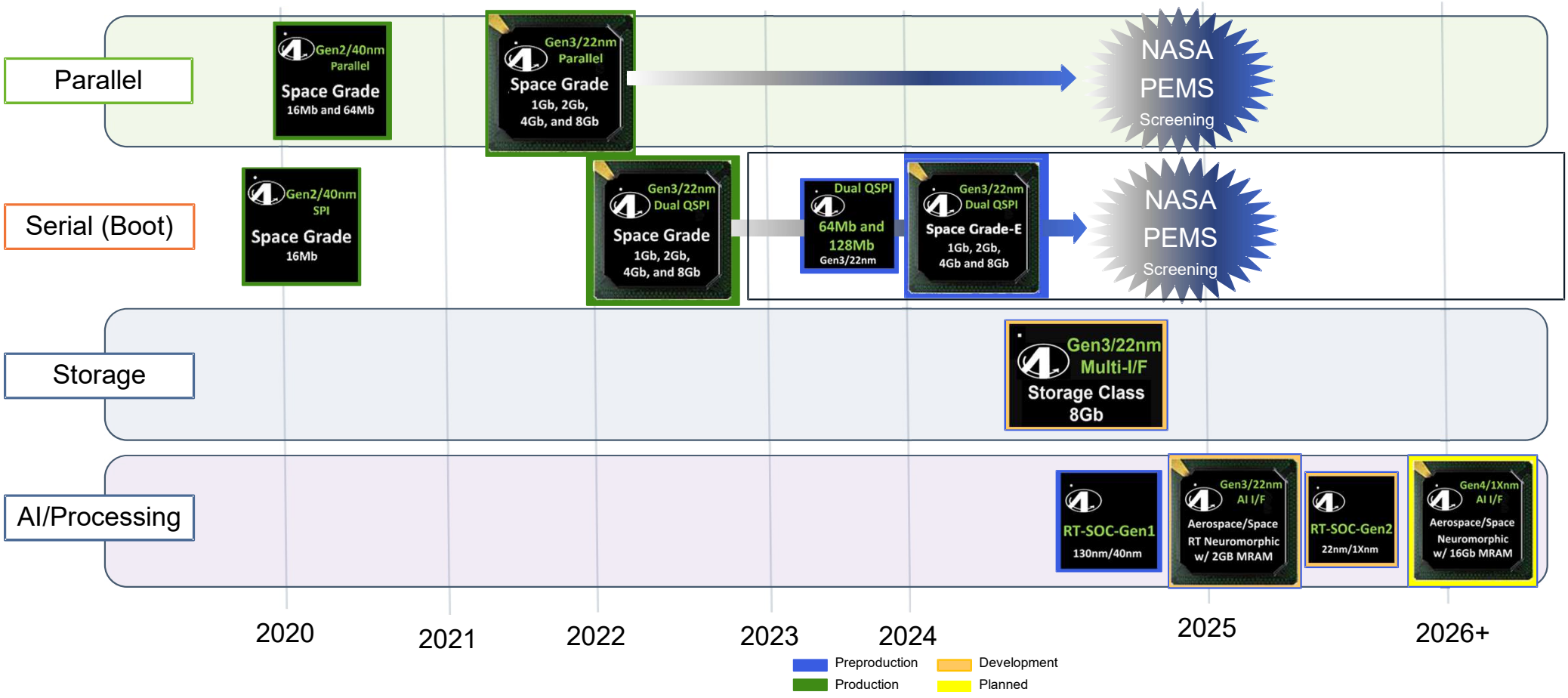
Roadmap Update
De-Risking Each Space Mission
Avalanche offers the only reliable, scalable, and low power memory solutions for satellites, rocket missions, and data centers in space.
Boot Memory
Storage
AI Multi-

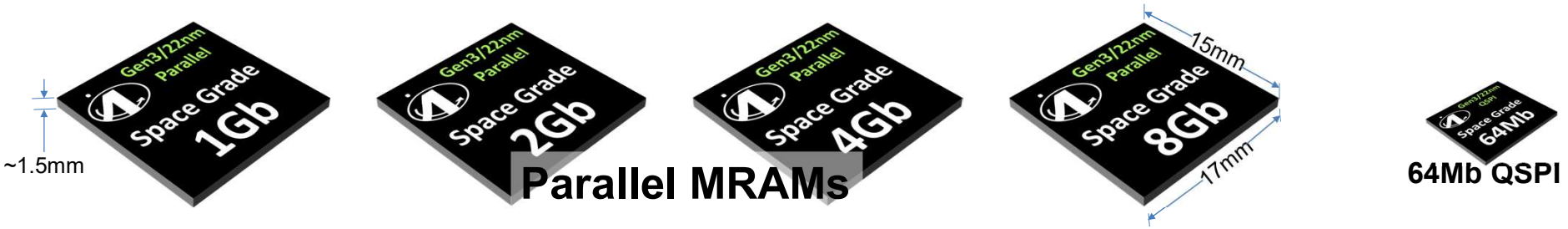
Avalanche MRAM/Processing Product Roadmap



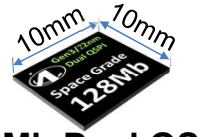
Avalanche MRAM/Processing Product Roadmap



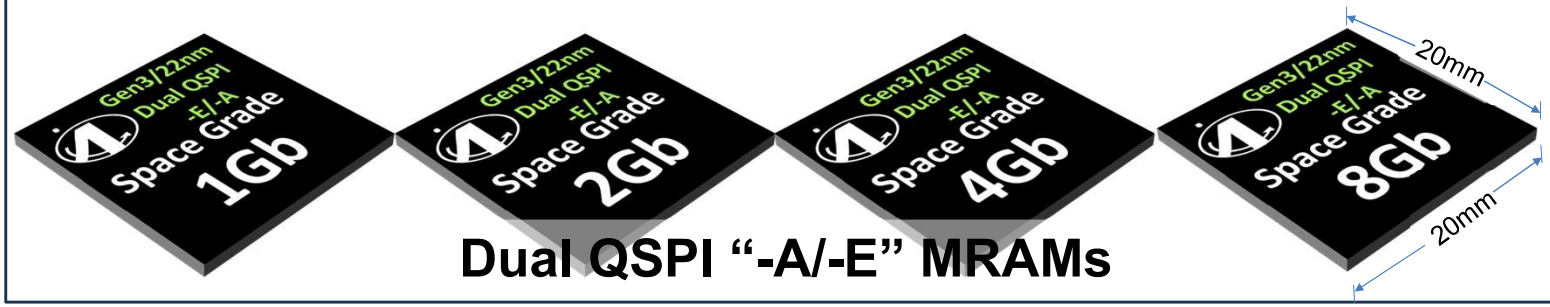
Avalanche Family of Gen3 MRAM Devices



64Mb QSPI



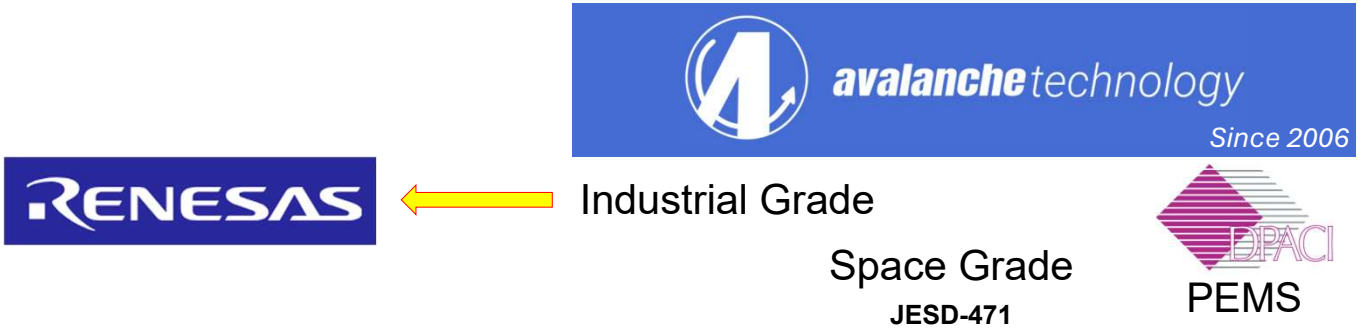
128Mb Dual QSPI



-A/-E has Higher:

- **TID and SEE**
- **Performance and**
- **An Extended SOA**

Powered by Avalanche – MRAM Device Ecosystem



micross
one source. one solution.®

Space Grade
QED, PEMS, QML, and RadHard
30-year Hi-Rel Qual Heritage
Plastic, Die, Hermetic, and MCM

FRONTGRADE

Space Grade
QED, PEMS, and RadHard
Standard and Custom
30-year Qual Heritage

Radiation Results for Gen3 Family

Dual QSPI

RADIATION TEST SOLUTIONS

In support of:

Avalanche Technology, Inc

AVALACHE DUAL-QSPI STT-MRAM WITH 65NM INTERFACE CHIPLET HEAVY ION SEE TEST REPORT

RTS24-I0341-02TR-F

10/2/2024

620 Years

TABLE 0-2. HCE AND SHUTDOWN RATE CALCULATIONS.
(5-YEAR GEO OR 1 AU ORBIT, 0.100" AL SHIELDING)

Error Mode	Event/Device/Day	Years/Event
HCE and Shutdown Fit	4.4E-06	6.2E+02

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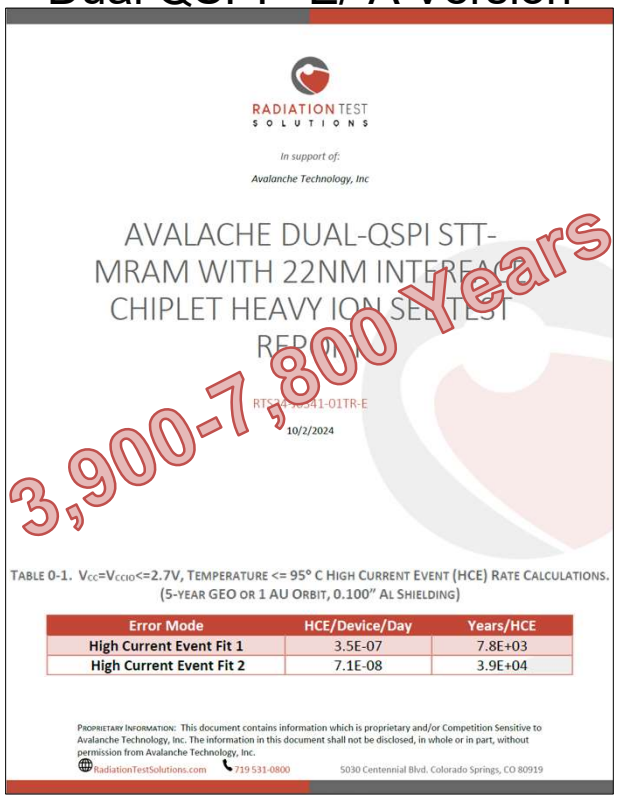
Dual QSPI –E/-A Version



RADIATION TEST SOLUTIONS

In support of:

Avalanche Technology, Inc

AVALACHE DUAL-QSPI STT-MRAM WITH 22NM INTERFACE CHIPLET HEAVY ION SEE TEST REPORT

RTS24-I0341-01TR-E

10/2/2024

3,900-7,800 Years

TABLE 0-1. V_{CC}=V_{CCIO}<=2.7V, TEMPERATURE <= 95° C HIGH CURRENT EVENT (HCE) RATE CALCULATIONS.
(5-YEAR GEO OR 1 AU ORBIT, 0.100" AL SHIELDING)

Error Mode	HCE/Device/Day	Years/HCE
High Current Event Fit 1	3.5E-07	7.8E+03
High Current Event Fit 2	7.1E-08	3.9E+04

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Parallel and 64Mb/128Mb Gen3 Devices are scheduled at LBNL this month

With Volumes Comes Reliability

Total MRAM Devices Shipped = **1,439,946**

Total MRAM Terabits Shipped = **26.598 Tbits**

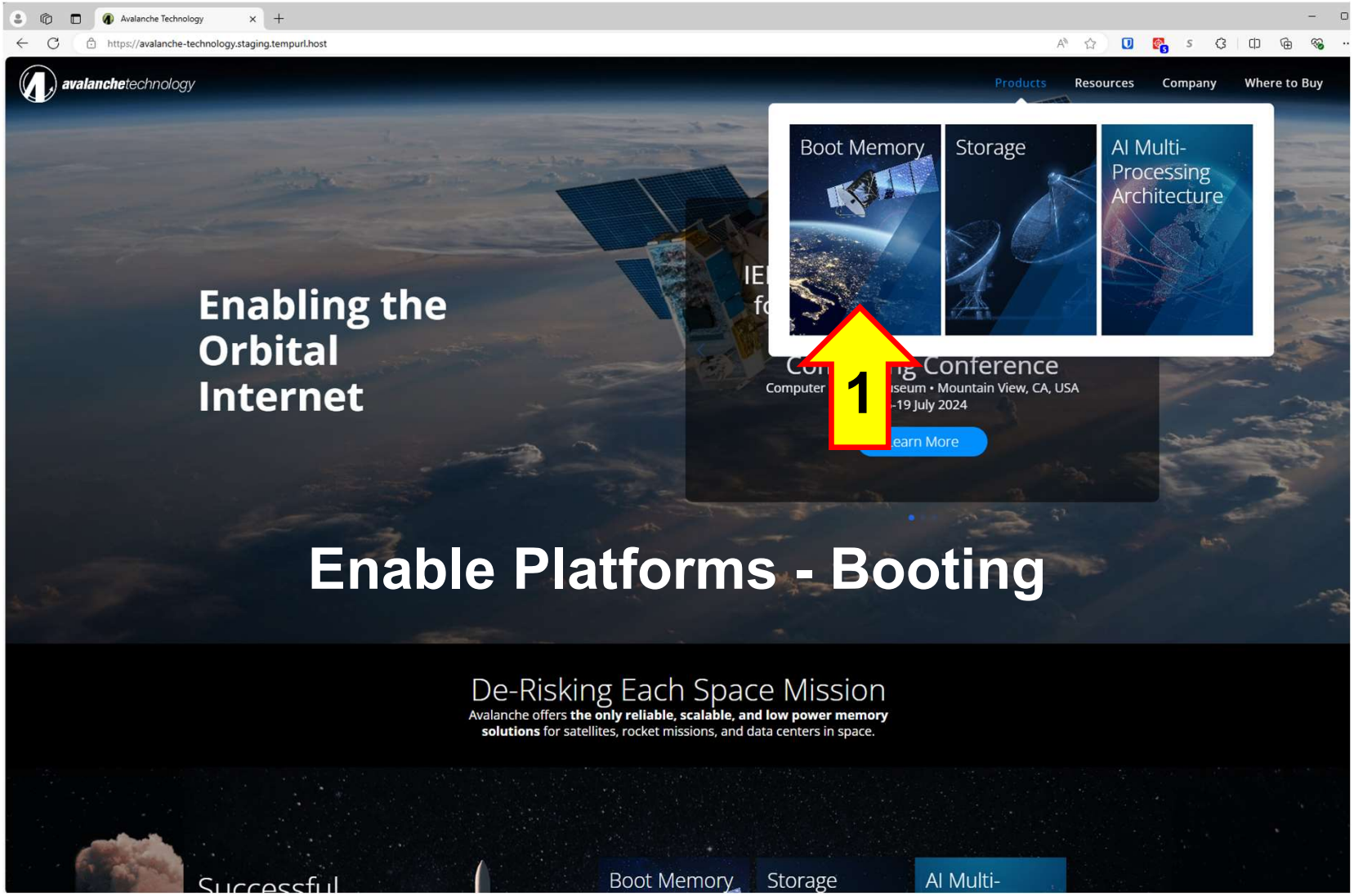
Industrial Devices = **1,428,991**

Industrial Terabits = **13.120 Tbits**

Space Grade Devices = **10,755**

Space Grade Terabits = **13.478 Tbits**

To put that in perspective, it would take 220K 64Mb Legacy MRAMs to store 13.5 Tbits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Avalanche offers the only reliable, scalable, and low power memory solutions for satellites, rocket missions, and data centers in space.
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Hi-Rel Boot Requirements are Only Increasing: 64Mb to ~1Gb per image

Type	Vendor	Device	Density
FPGA	AMD/Xilinx	Virtex-4QV -XQR4V	64 Mb
		Virtex-5QV -XQR5V	64 Mb
		RT KintexUltrascale-XQRKU060	256 Mb
		ZynqUltrascale+	256 Mb
		ZynQ UltraScale+ (ZCZU15)	≥ 512 Mb
		Versal-XQRV	≥ 1 Gb
	Microchip	RT Polarfire RTPF500T-1CB1509	118 Mb
	Lattice	CertusPro	128 Mb
	Frontgrade	CertusPro RT UTC24CP1008	128 Mb
SoC		SoC UT32M0R500	64 Mb
		Gaisler GR716B	64 Mb
	Vorago	ARM-M4 VA41629	64 Mb

Higher Density ROMs required

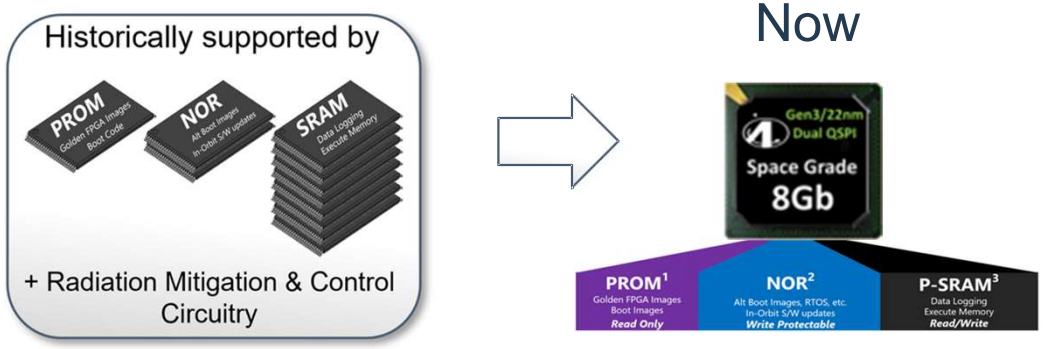
- Full PetaLinux – including User Applications
- Large FPGAs/MPSoCs
  - UltraScale, UltraScale+, Versal, MPSoC, CertusPro, Polarfire, etc.

Configuration Memory Data Integrity from start until end of mission

- Data Retention
- Non-Volatile
- SEL Immunity
- SEU Immunity
- High Endurance

Enabled Booting and nvStorage for AMD/Xilinx Devices

SW-Defined Platforms for Space – Respond to Threats in Real Time



No redundancy, mitigation or control needed

Dramatically simplified hw & sw architecture, rapid boot

In Orbit FOTA support: multi-mission adaptability ENABLED

Support Resources Available

Family	Petalinux Support				Fabric Only
	23.2	23.1	22.2	22.1	No O/S
Versal	✓	✓	✓	✓	✓
Ultrascale+	✓	✓	✓	✓	✓
Ultrascale	✓	✓	✓	✓	✓

https://www.avalanche-technology.com/support/development-kits/

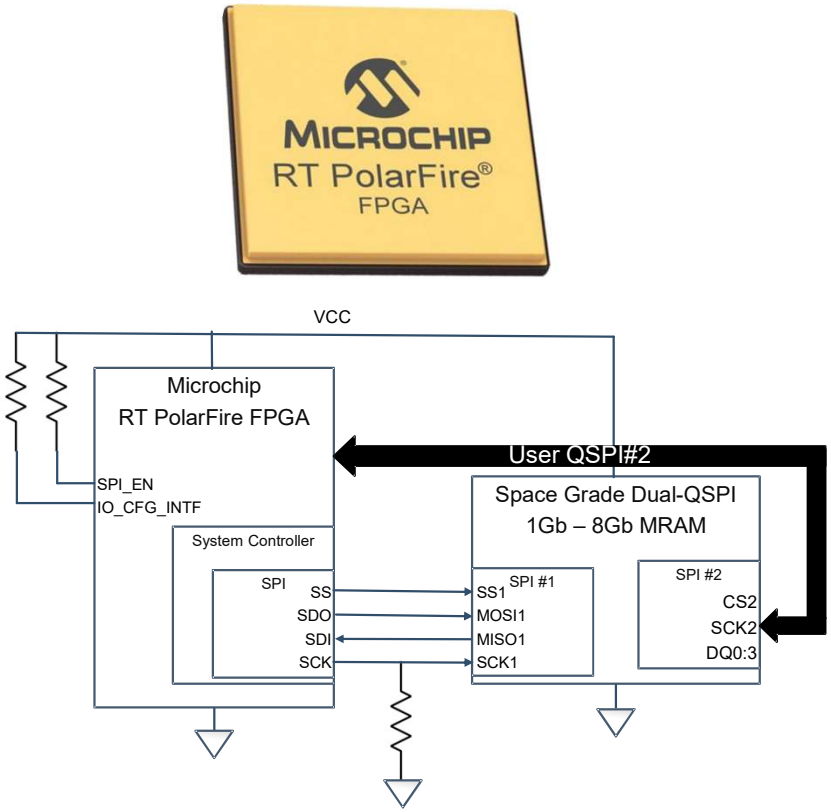
Gen 3 Space Grade Dual QSPI P-SRAM™ Kit for Xilinx

Development Kit:
Download the User Guide
Download the Sample Code
Xilinx/AMD Versal Boot Linux Drivers

Reference Design:
Download the Schematic, Board Layout, Gerber, BOMs

Orderable Part Numbers:
Kit: AK30X208XILCCSOC
Socket: ABGA96-1-20×20

Enabled auto-updating RT PolarFire's on-board Flash



Auto-updating RT PolarFire FPGAs w/MRAM

RT PolarFire use SFDP [Serial Flash Discoverable Parameters]. Part of the JESD216 standard.

Avalanche DQSPI MRAMs do not support SFDP.

However, Avalanche DQSPI MRAMs have successfully auto-updated the RT PolarFire's on-board flash using its extended address register.

Reliable Booting for Vorago ARM-M4 Series Family SoCs

VA41630

RH ARM M4 MCU

VA7230

RT Edge Processing MPU

Config Bit Stream

Serial I/F

Pin Compatible Boot Solutions

Compact Images
10x10mm FBGA

Dual QSPI
64Mb and 128Mb
Gen3/22nm

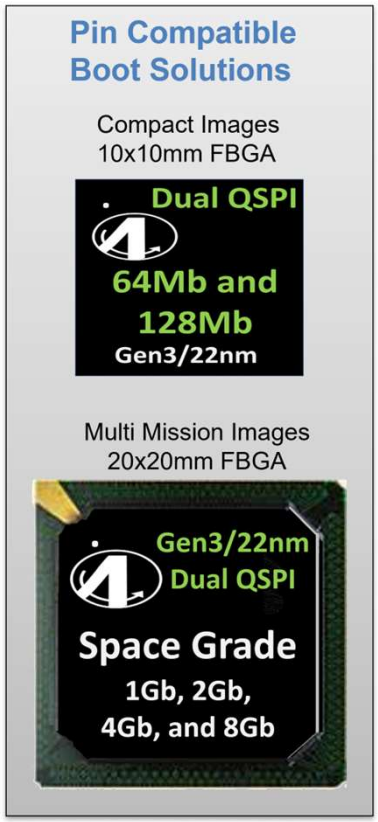
Multi Mission Images
20x20mm FBGA

Gen3/22nm
Dual QSPI
Space Grade
1Gb, 2Gb, 4Gb, and 8Gb

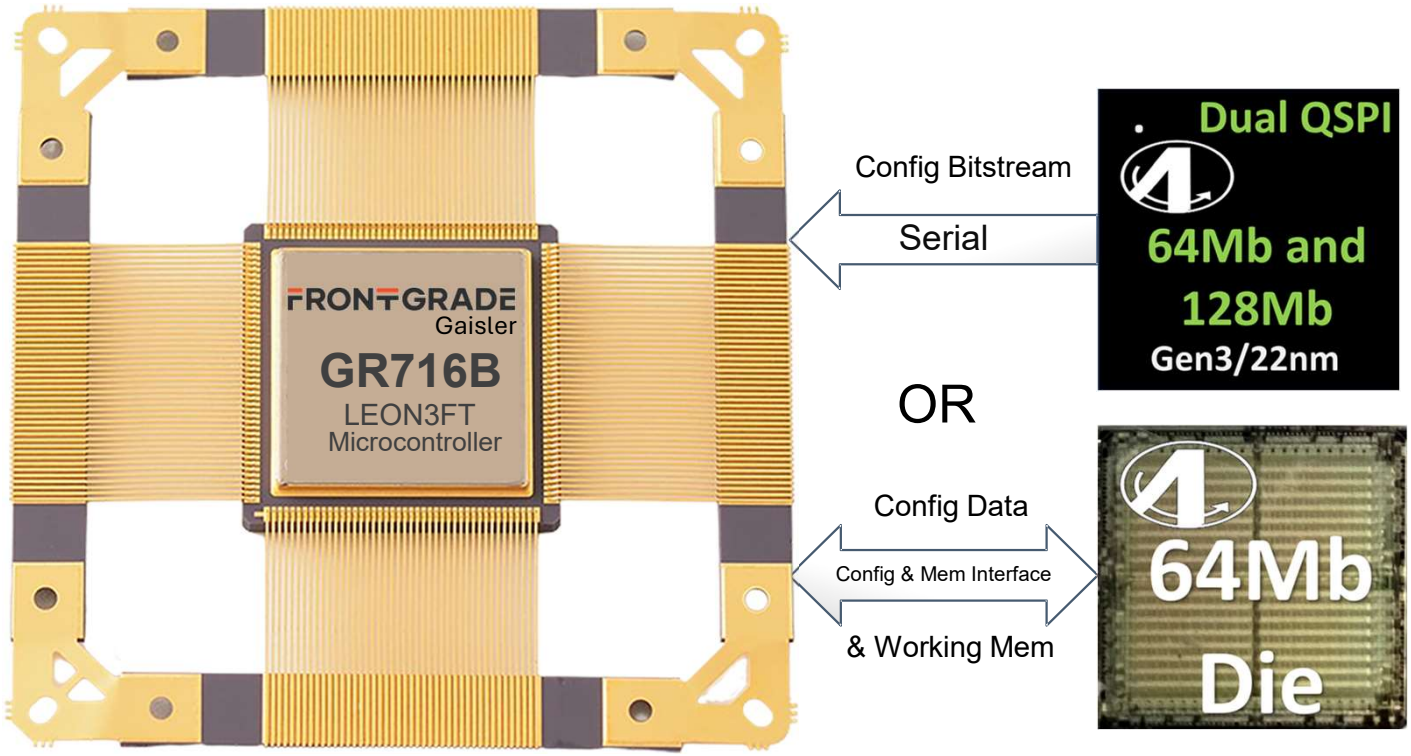
Enabling Booting for Frontgrade/Lattice CertusPro FPGAs & UT32M0R500 SoC

Config Bit Stream

Serial I/F



Enabling Booting & Working Memory for Gaisler GR716 LEON3FT Processor



Advanced Boot Solutions Enabling SW-Defined Platforms

Avalanche Technology Announces Support for NASA PEMS Qualification and Screening

In response to unprecedented demand for extended quali
compatible NASA PEMS options for enabling Dual QSPI M

FREMONT, CA, April 8, 2024 — Avalanche Technology, the leader in next generation MRAM technology, announced today the launch of a new product derivative to address the growing demand from the aerospace and defense community for extended qualification and screening solutions, particularly NASA PEMS INST-0001.

Leveraging Avalanche's Gen 3 Space Grade MRAM products being broadly adopted by the defense industrial base and commercial space customers, the new pin compatible PEMS qualified and screened versions of the popular Dual QSPI MRAMs will roll out mid-year.

Avalanche Technology Selected to Support Mercury's First Space-Qu
Processing Board Using AMD's Xilinx Versal AI Core

mercury systems™

oducts to build the next family of SWaP optimize

FREMONT, Calif., Nov. 8, 2023 /PRNewswire-PRWeb/ — Avalanche Technology, the leader in next generation MRAM technology, announced today that its Persistent-SRAM (P-SRAM) products were by Mercury Systems for the new SCFE6933, a next-generation processor board that will enable fa processing of data in orbit. The high-density 8Gb DQSPI Space Grade Persistent SRAM with furthe scalability is the ideal companion to the AMD (Xilinx) Versal Adaptive SoC platform that is feature platform.

What Are Our Customers Saying…

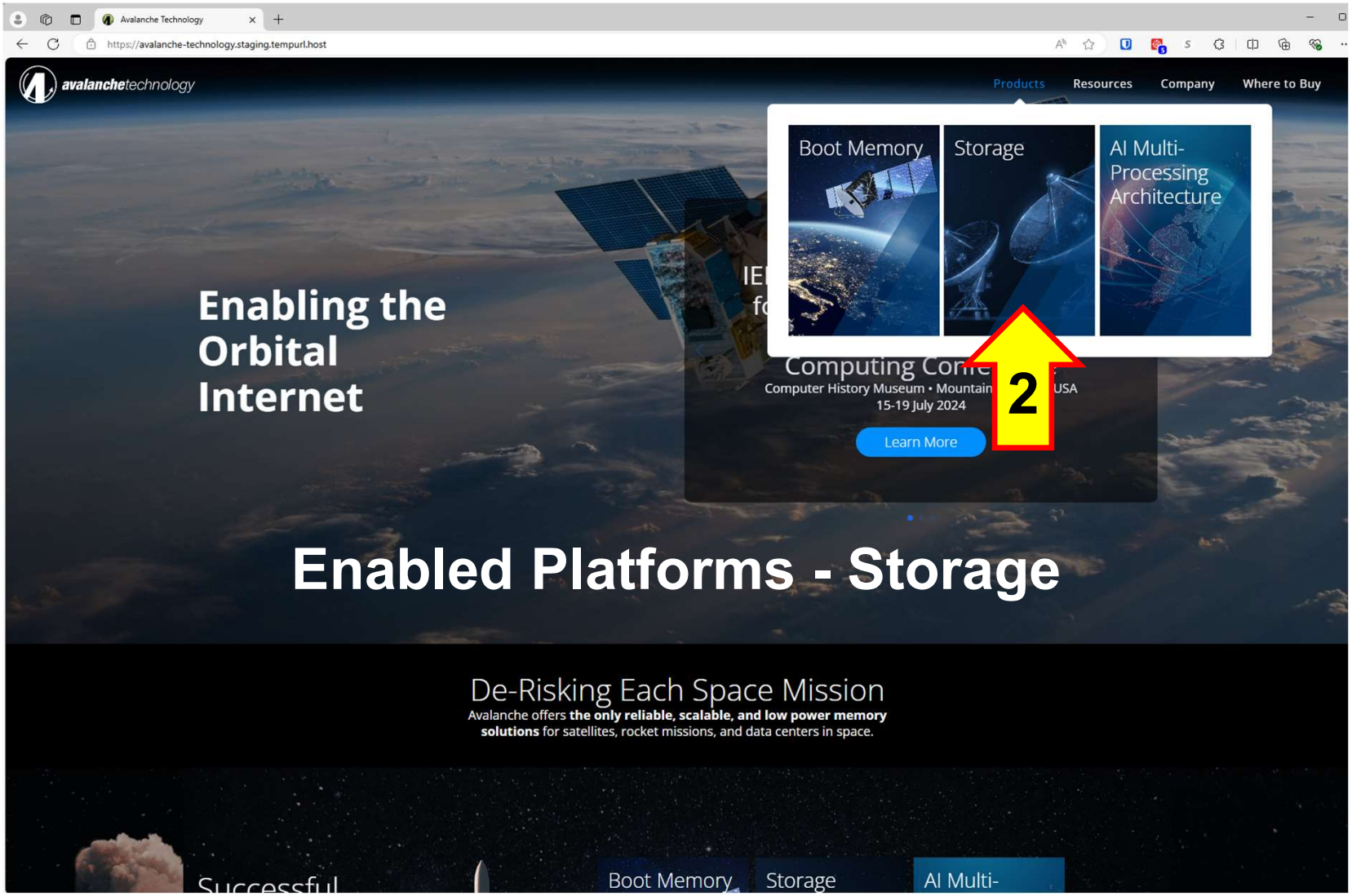
Your Memory is being used on every platform for every satellite we have planned for flight.
Senior Member of Quality/TIB, July 2024

Avalanche is now my first call when I need memory after integrating it into our last successful program.
Lead Electrical Engineer, Jan 2024

Avalanche MRAM is now our memory of choice throughout GD for all space programs
Chief Technologist, August 2024

Avalanche was able to get us out of a real problem in meeting our radiation requirements where your competition could not, allowing us to move forward on our programs.
Reliability Manager, March 2024

Having ecosystem partners like Avalanche support multiple mission images and FOTA for AMD adaptive SoC platforms helps ensures ultimate versatility for changing mission requirements.
Minal Sawant, senior director of Aerospace and Defense Vertical Market, AMD, Jan 2024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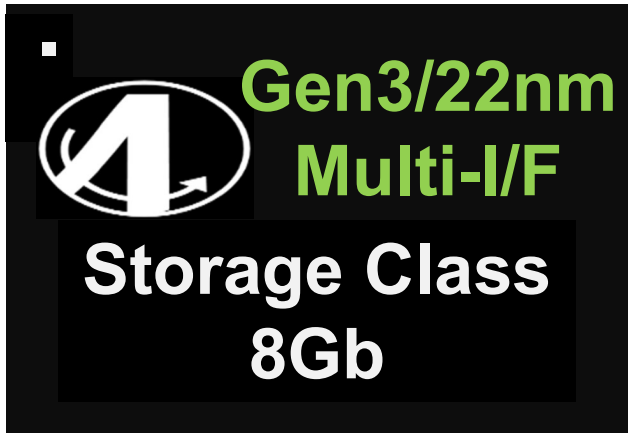
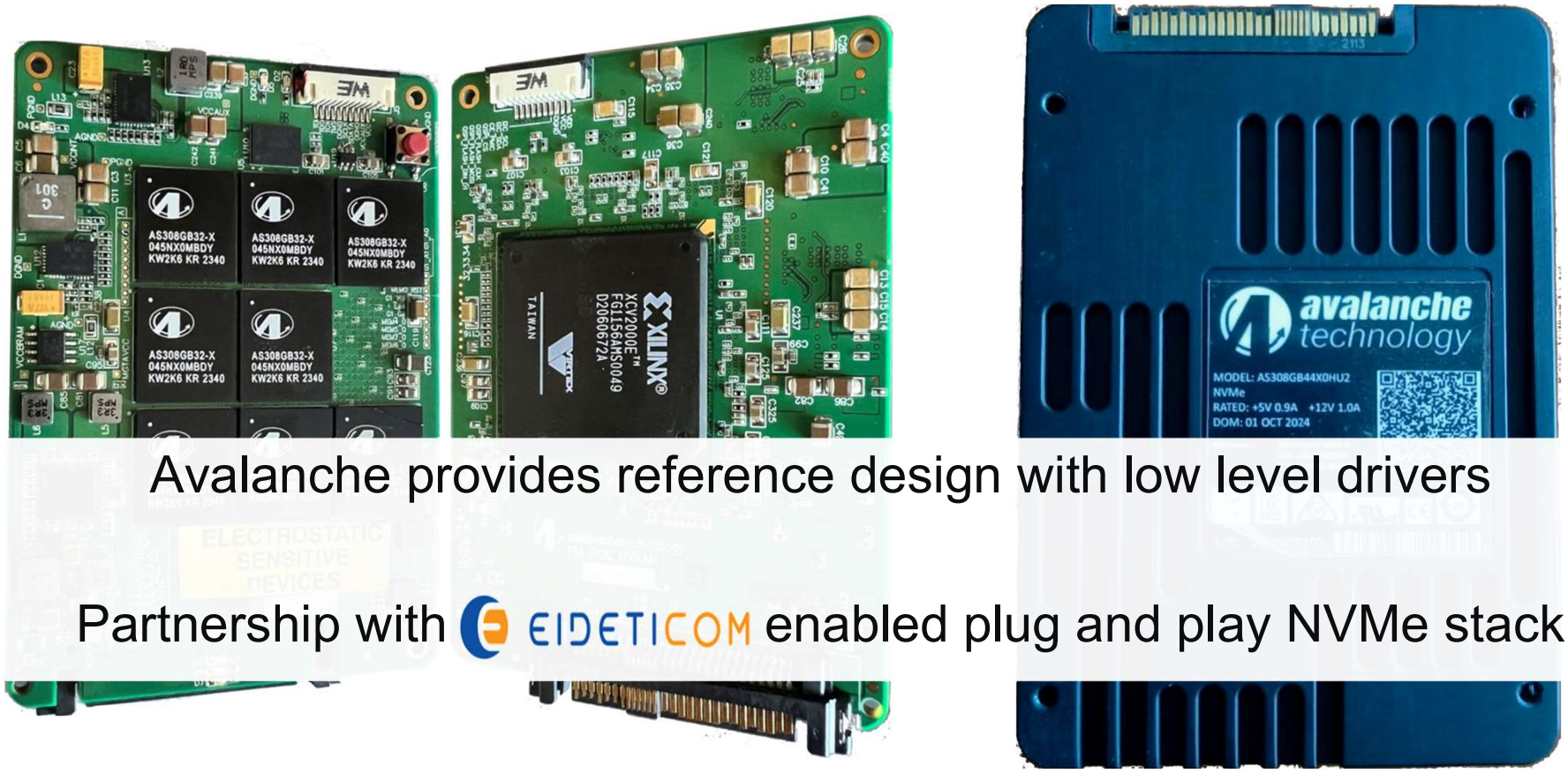
Avionics and Space Grade Storage Class Solutions



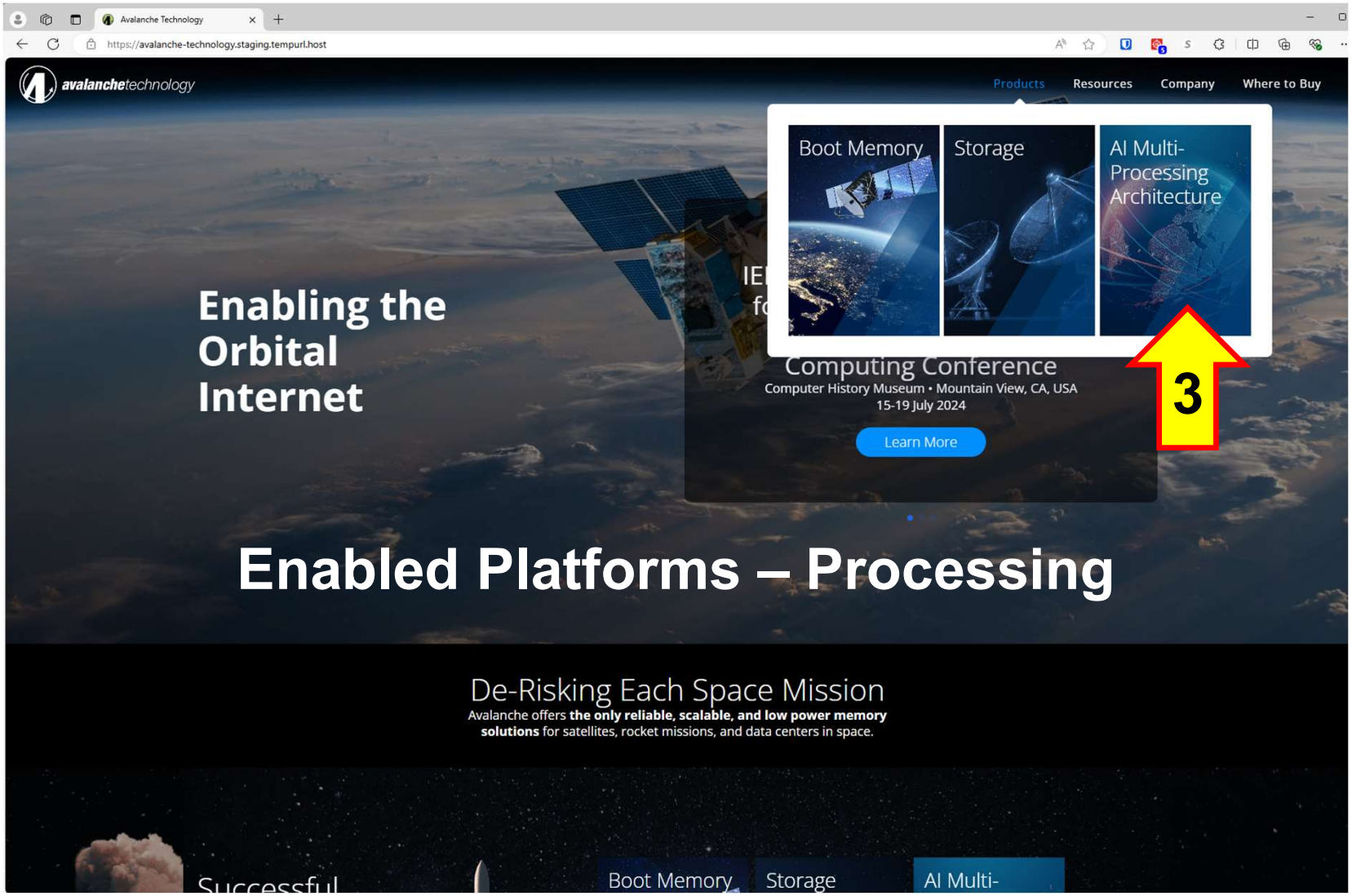
Standard M.2 module is available as an evaluation card and as a reference design

Enabling the driver for Storage Solutions in Space



Avalanche provides reference design with low level drivers

Partnership with EIDETICOM enabled plug and play NVMe stack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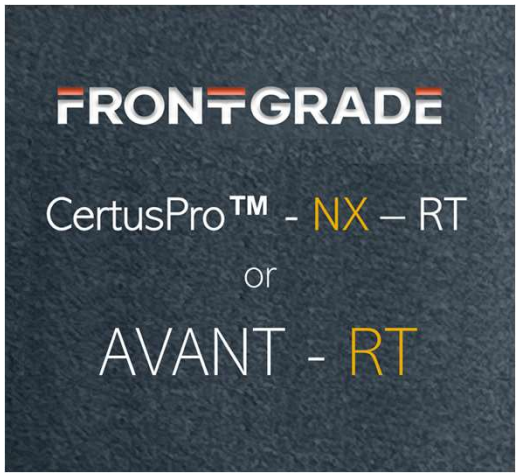
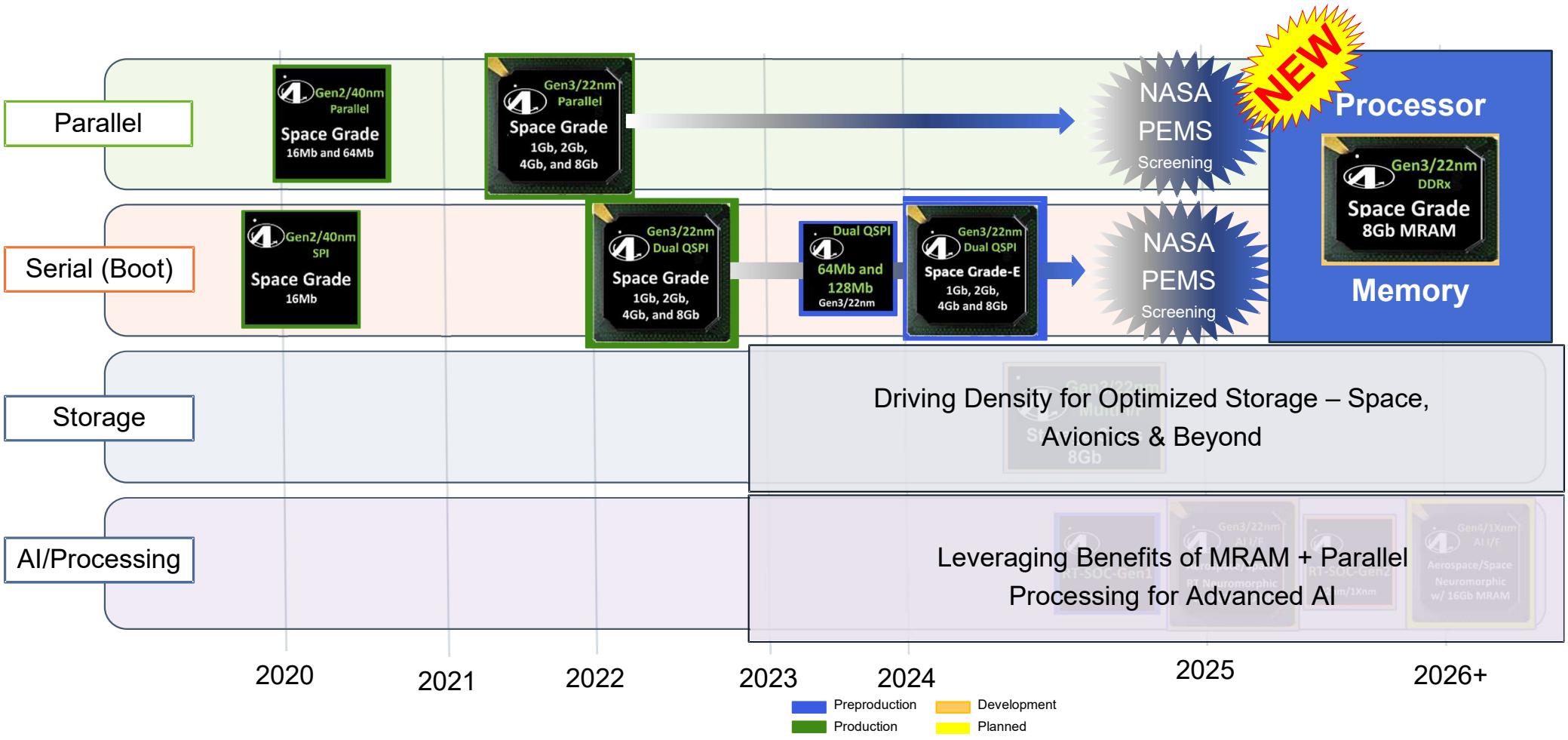
Popular Hi-Rel/Space Processors…



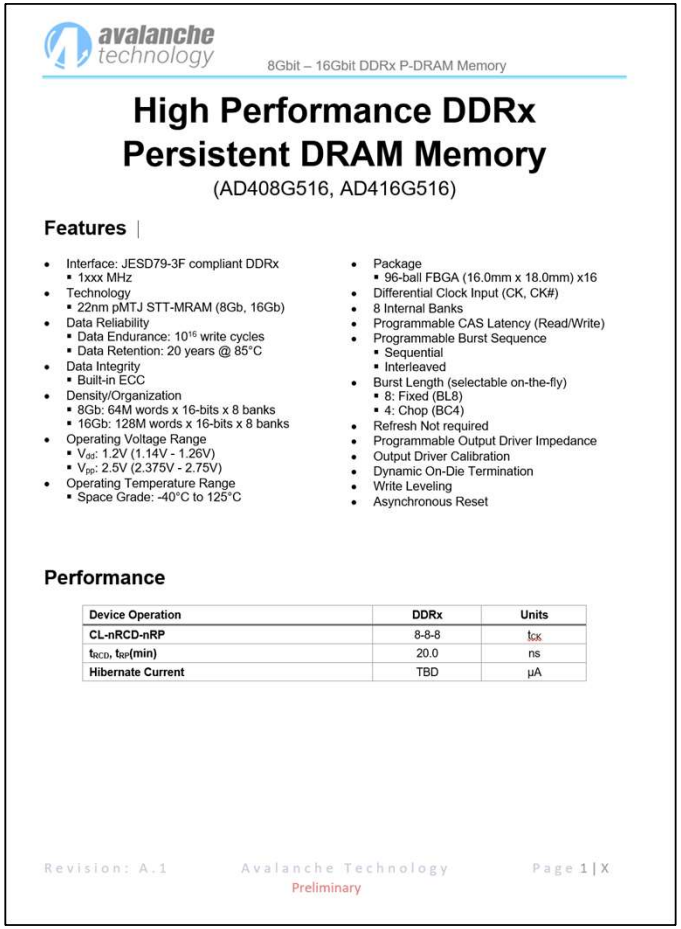
…All Use DDRx DRAM Memory as Processing Memory

Avalanche MRAM's "Instant ON" capability would make an ideal choice

Avalanche MRAM/Processing Product Roadmap Update



Introducing Avalanche's DDRx Persistent DRAM



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8Gbit – 16Gbit DDRx P-DRAM Memory

High Performance DDRx Persistent DRAM Memory

(AD408G516, AD416G516)

Features

- Interface: JESD79-3F compliant DDRx
  - 1xxx MHz
- Technology
  - 22nm pMTJ STT-MRAM (8Gb, 16Gb)
- Data Reliability
  - Data Endurance: 10^{16} write cycles
  - Data Retention: 20 years @ 85°C
- Data Integrity
  - Built-in ECC
- Density/Organization
  - 8Gb: 64M words x 16-bits x 8 banks
  - 16Gb: 128M words x 16-bits x 8 banks
- Operating Voltage Range
  - V_{dd}: 1.2V (1.14V - 1.26V)
  - V_{pp}: 2.5V (2.375V - 2.75V)
- Operating Temperature Range
  - Space Grade: -40°C to 125°C
- Package
  - 96-ball FBGA (16.0mm x 18.0mm) x16
- Differential Clock Input (CK, CK#)
- 8 Internal Banks
- Programmable CAS Latency (Read/Write)
- Programmable Burst Sequence
  - Sequential
  - Interleaved
- Burst Length (selectable on-the-fly)
  - 8: Fixed (BL8)
  - 4: Chop (BC4)
- Refresh Not required
- Programmable Output Driver Impedance
- Output Driver Calibration
- Dynamic On-Die Termination
- Write Leveling
- Asynchronous Reset

Performance

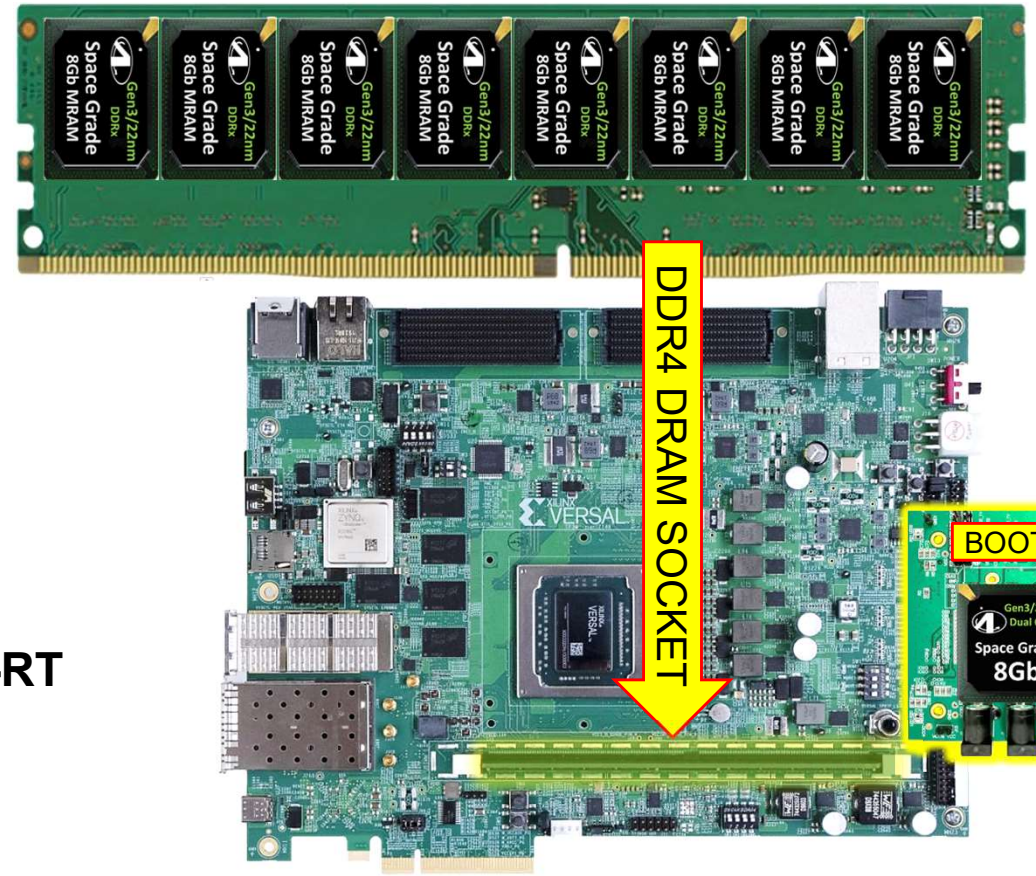
Device Operation	DDRx	Units
CL-nRCD-nRP	8-8-8	t_{CK}
t_{RCD}, t_{RP}(min)	20.0	ns
Hibernate Current	TBD	µA

Revision: A.1 Avalanche Technology Page 1 | X

Preliminary

- **Leverage chiplet-based design to mitigate risk**
- **Chiplet based on same RHBD rules as MRAM die**
- **1Gb MRAM has flight heritage**
- **Funded Project / On-going Development**

8GByte DDRx Persistent DRAM DIMM for Standard Development Kits



Target Development Systems:

- **AMD/Xilinx Versal** (VCK190)
- **AMD/Xilinx KU060** (ZCU106)
- **Lattice/Frontgrade CertusPro-RT**
- **Lattice/Frontgrade Avant-RT**

Note: 8GByte P-DRAM DIMM is for Development Purposes ONLY

Thank You!

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